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Miller

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(54) **TESTER CHANNEL TO MULTIPLE IC TERMINALS**

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(52) **U.S. Cl.** 324/754; 324/765
(58) **Field of Search** 324/754, 757–758, 324/760, 762, 765, 158.1; 714/724, 734, 738, 742; 333/33, 246–247; 702/85–89, 104–119

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(57) **ABSTRACT**

A probe card provides signal paths between integrated circuit (IC) tester channels and probes accessing input and output pads of ICs to be tested. When a single tester channel is to access multiple (N) IC pads, the probe card provides a branching path linking the channel to each of the N IC input pads. Each branch of the test signal distribution path includes a resistor for isolating the IC input pad accessed via that branch from all other branches of the path so that a fault on that IC pad does not substantially affect the voltage of signals appearing on any other IC pad. When a single tester channel is to monitor output signals produced at N IC pads, the resistance in each branch of the signal path linking the pads of the tester channel is uniquely sized to that the voltage of the input signal supplied to the tester channel is a function of the combination of logic states of the signals produced at the N IC pads. The tester channel measures the voltage of its input signal so that the logic state of the signals produced at each of the N IC output pads can be determined from the measured voltage.

21 Claims, 6 Drawing Sheets
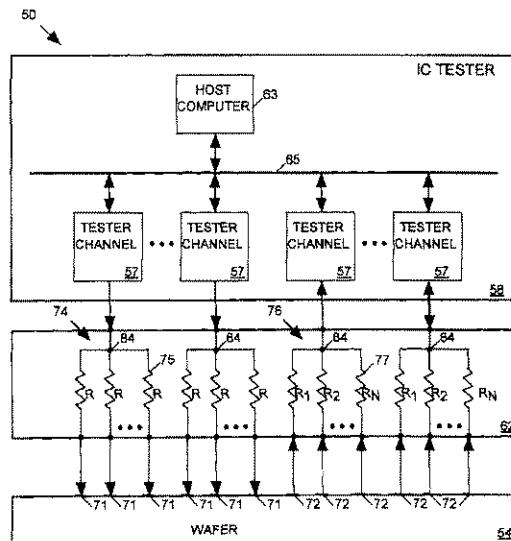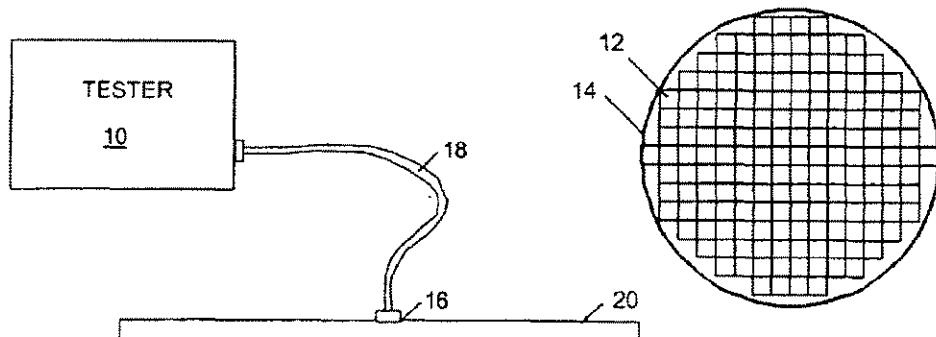
FIG. 1
(PRIOR ART)

FIG. 2
(PRIOR ART)

FIG. 3
(PRIOR ART)
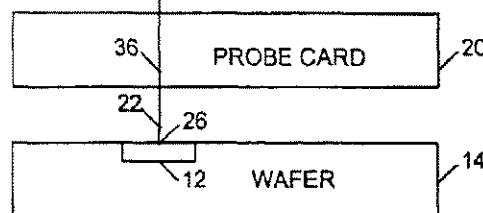
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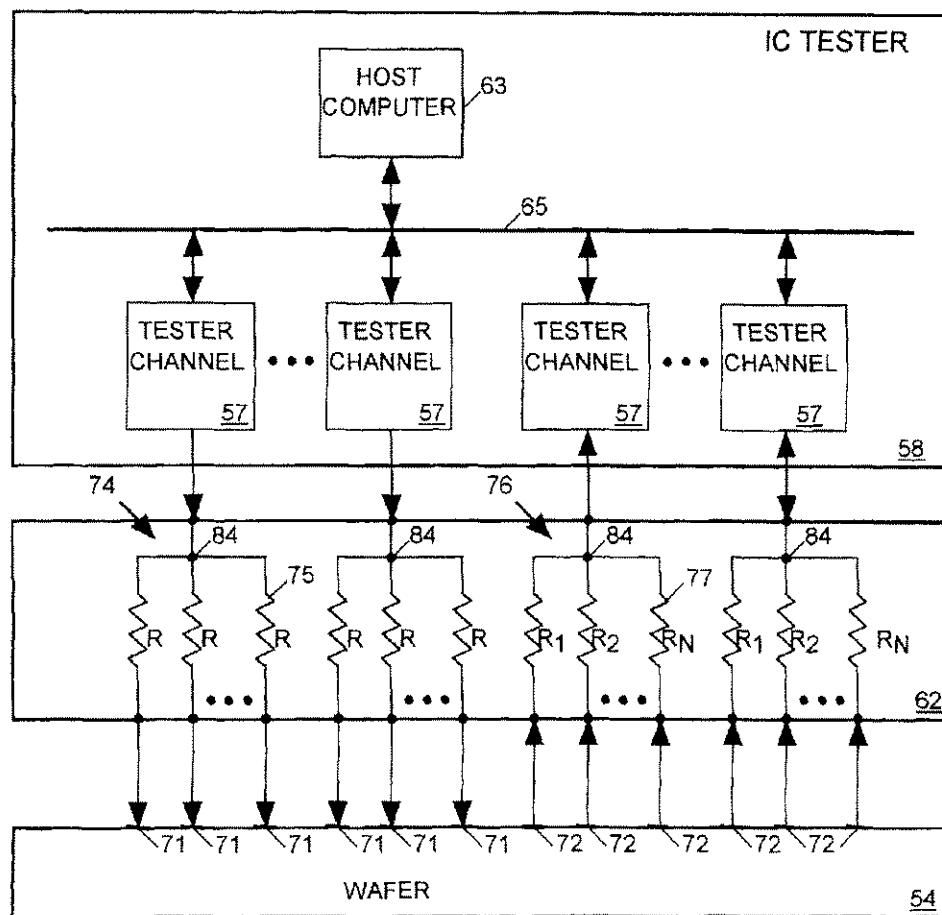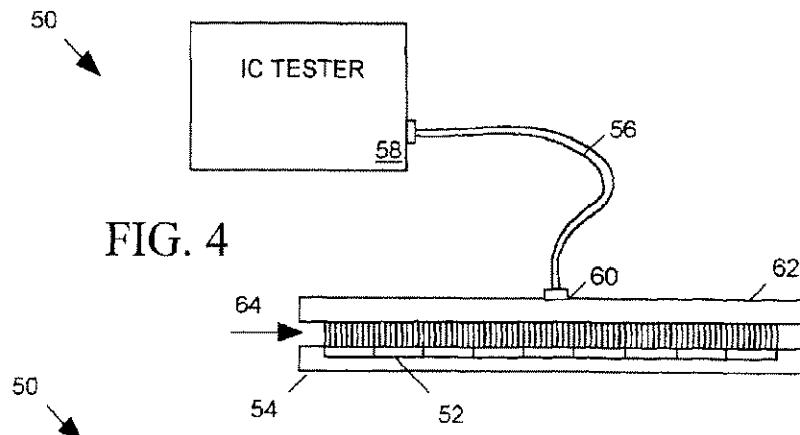
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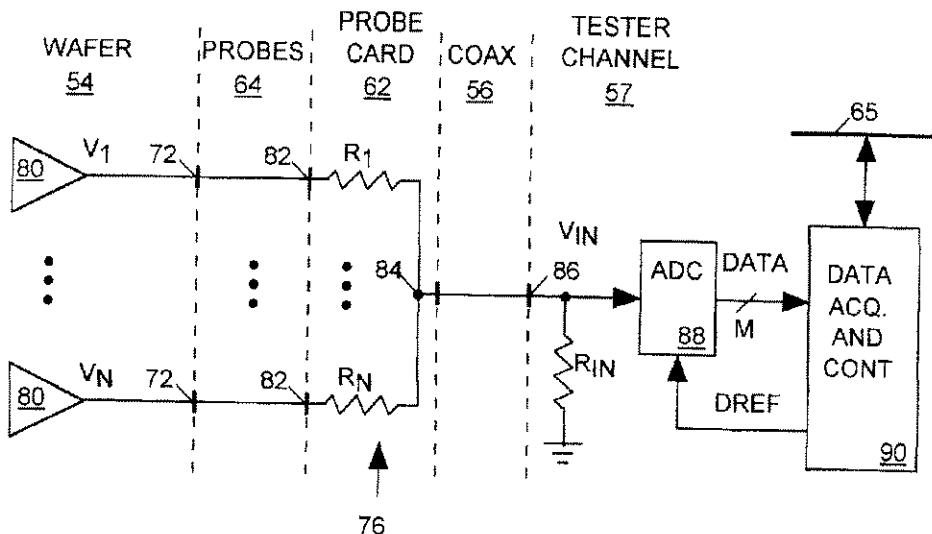
FIG. 6

FIG. 7

FIG. 8

FIG. 9

FIG. 10

$R_1 = 100\Omega$

V_1

$R_2 = 50\Omega$

V_2

V_{IN}

$R_3 = 25\Omega$

V_3

FIG. 11

V_{IN}

95

VREF

94(1)

DAC

96

94(2)

DAC

CDAT

94(M)

DAC

DREF
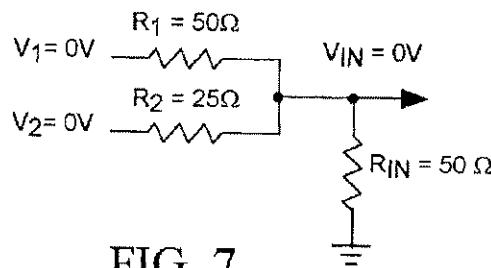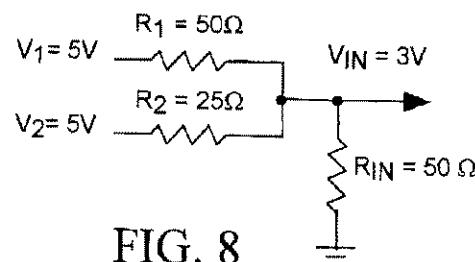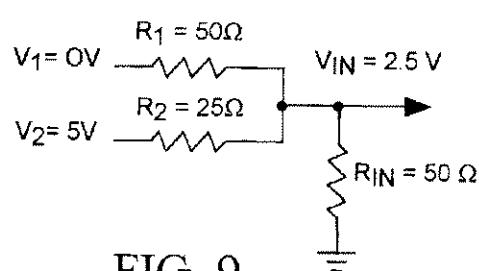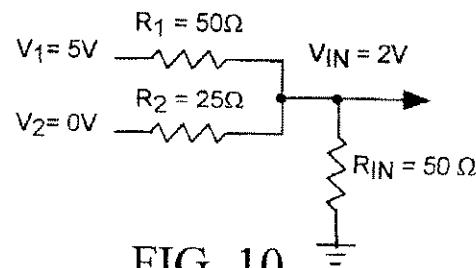
FIG. 12
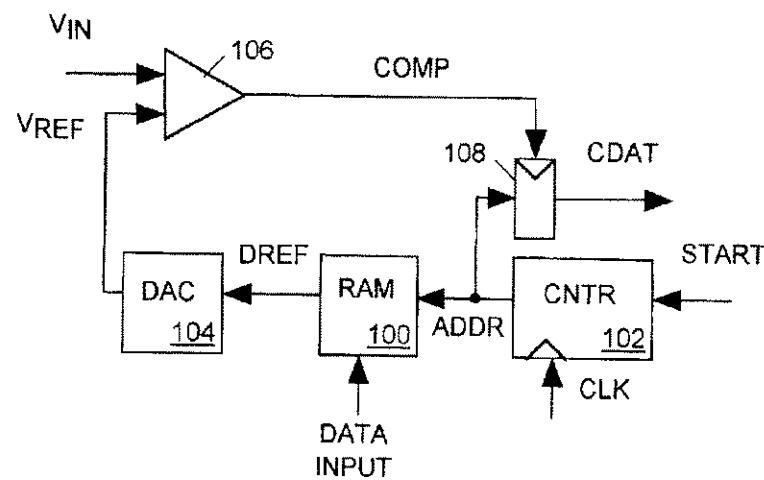
FIG. 13
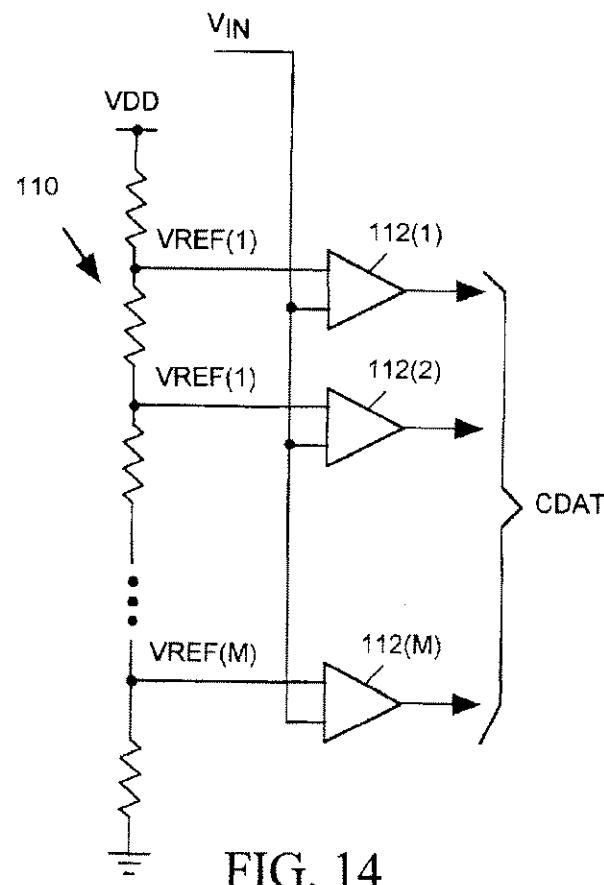
FIG. 14
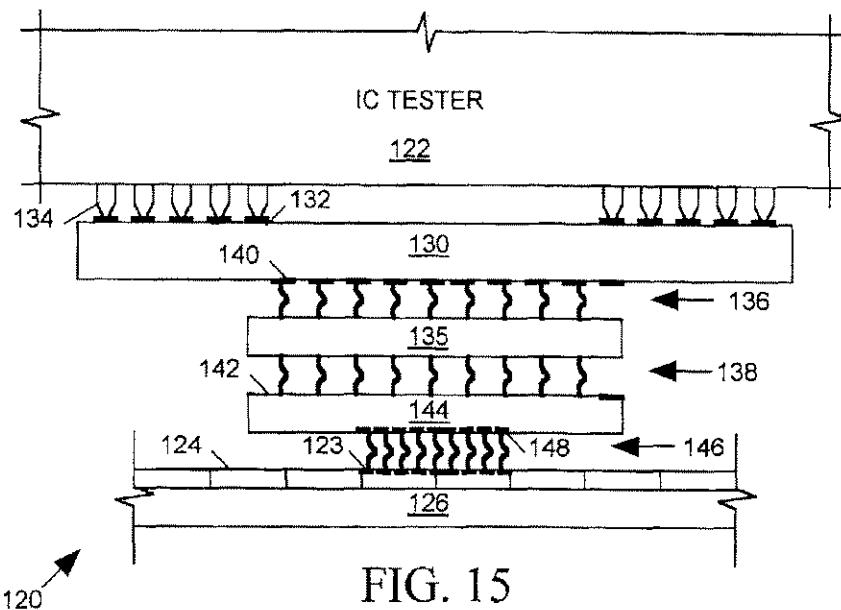
FIG. 15
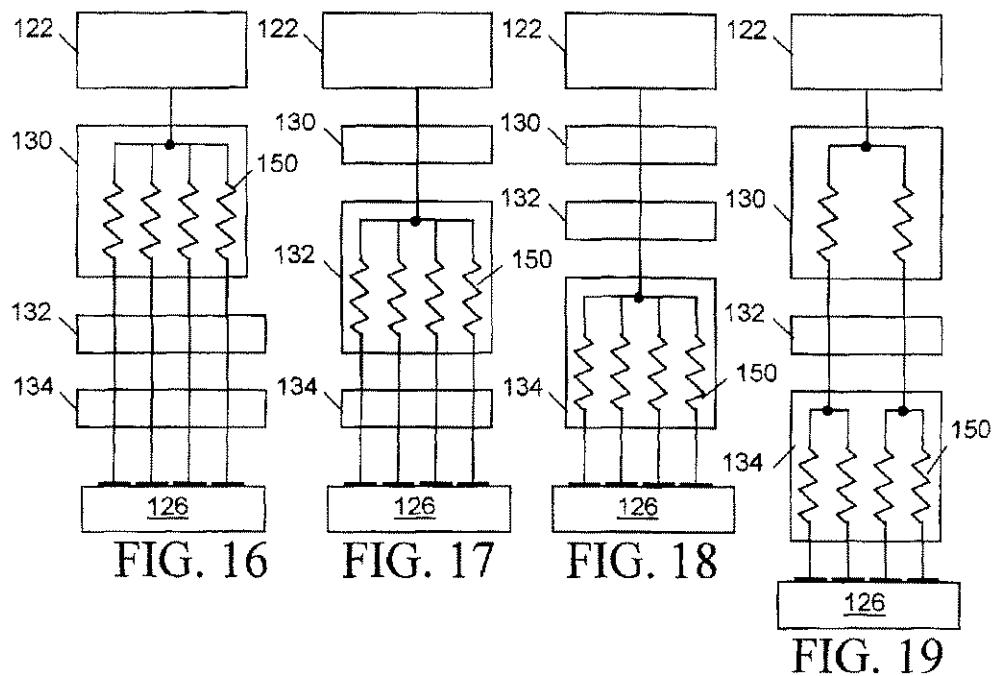
FIG. 16

FIG. 17

FIG. 18

FIG. 19

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<div style="display:flex;justify-content:space-between">12</div>

TESTER CHANNEL TO MULTIPLE IC TERMINALS

FIELD OF THE INVENTION

The invention relates in general to systems for testing integrated circuits (ICs), and in particular to a system for distributing a single test signal output of an IC tester to multiple input terminals of one or more ICs and for determining states of output signals produced at multiple IC output terminals.

DESCRIPTION OF RELATED ART

As illustrated in FIG. 1, an integrated circuit (IC) manufacturer fabricates an array of ICs 12 on a semiconductor wafer 14 and then cuts the wafer to separate the ICs from one another. The manufacturer may then install the ICs in separate packages using bond wires to link the IC's input/output (I/O) terminals (conductive pads on the surface of each IC) to package pins providing signal paths to external circuits. Some ICs include "redistribution" layers covering its I/O terminals. Conductors within the redistribution layers link the IC's I/O terminals to contact pads formed on the top surface of the redistribution layers. The contact pads are larger than the IC's I/O terminals and are more evenly distributed so that the IC can be mounted directly on printed circuit boards (PCBs), for example by soldering the pads to correspondingly arranged contact pads on the surfaces of the PCBs. Spring contacts can also be used to link the IC's redistributed contact pads to a PCB's contact pads. The spring contacts may be formed either on the IC's contact pads or on the PCB's contact pads.

ICs may be tested at the wafer level before they are separated from one another or may be tested after they have separated. Referring to FIG. 2, an IC tester 10 for testing an array of ICs 12 residing on a wafer 14 (or for testing an array of singulated ICs held on a tray) typically includes a set of tester channels, each of which may either transmit a test signal to an IC input pad or monitor an IC output signal produced at an IC output pad to determine whether the IC responds correctly to its input signals. A set of coaxial cables 18 provides signal paths between the tester channels and a cable connector 16 on a probe board 20. A set of probes 22 link pads on the lower surface of probe board 20 to the redistribution or I/O terminal pads on the upper surfaces of ICs 12. Various types of structures can be used to implement probes 22 including, for example, wire bond and lithographic spring contacts, needle probes, and cobra probes. When spring contacts are used to implement probes 22 they may be formed either on pads on the upper surfaces of ICs 12 or on pads on the lower surface of probe board 20.

U.S. Pat. No. 6,064,213, issued May 16, 2000 to Khandros et al., incorporated herein by reference, discloses an example of a card assembly designed to contact spring contacts formed on an IC. U.S. patent application Ser. No. 09/810,871 filed Mar. 16, 2001 (incorporated herein by reference) describes another example of a card assembly employing spring contact probes. U.S. Pat. No. 5,974,662 issued Nov. 2, 1999, issued to Eldridge et al., incorporated herein by reference, describes an example of a probe card assembly in which spring contacts formed on a probe card function as probes. The following documents (incorporated herein by reference) disclose various exemplary methods for manufacturing spring contacts: U.S. Pat. No. 6,333,269 issued Jan. 8, 2002 to Eldridge et al., U.S. Pat. No. 6,255,126 issued Jul. 31, 2001 to Mathieu et al., U.S. patent application

Ser. No. 09/710,539 filed Nov. 9, 2000, and U.S. patent application Ser. No. 09/746,716 filed Dec. 22, 2000.

Probe board 20 is typically a multiple layer printed circuit board (PCB) providing signal paths between cable connector 16 and the pads on its lower surface. Traces formed on the various layers of probe board 20 convey signals horizontally while vias convey signals vertically though the layers.

Tester 10 typically provides a separate channel for each pad 26 that is linked to an I/O terminal of an IC to be tested. FIG. 3 illustrates one channel 24 of a typical tester accessing a pad 26 of a wafer 14 via a path 36 through a probe card 20. A test is usually organized into a succession of test cycles of uniform duration, and during each test cycle channel 24 may either provide an input to a pad 26 of an IC 12 formed on wafer 14 or may monitor an IC output signal produced by the IC at pad 26 to determine its state. A data acquisition and control circuit 30, programmed via instructions supplied through a bus 42, controls the action channel 24 is to carry out during each test cycle. When pad 26 is to receive an input signal, circuit 30 sets a tristate control input Z of a tristate driver 32 so that the driver supplies a test signal as input to pad 26. Circuit 30 sets an input signal D to driver 32 during each test cycle so that the test signal is of the correct logic state. The test signal travels to pad 26 through a signal path formed by one of cables 18, the signal path 36 provided by probe card 20, and one of probes 22.

When an IC 12 produces an output signal at pad 26, the output signal passes through probe 22, signal path 36 and cable 18 to become an input signal to a pair of comparators 38 and 39 within channel 24. Comparator 38 asserts a compare high (CH) signal when the voltage of IC output signal is higher than a high logic level threshold voltage produced by a digital-to-analog converter (DAC) 40. Comparator 39 asserts a compare low (CL) signal when the IC output signal voltage is lower than a low logic level threshold voltage produced by another digital-to-analog converter (DAC) 41. Circuit 30 supplies control data DREF as input to DACs 40 and 41 for controlling the voltage levels of the VH and VL reference signals.

For example, when the test signal has 5 volt and 0 volt high and low logic levels, the VH and VL threshold levels might be set to 4.5 and 0.5 volts, respectively, so that an IC output signal over 4.5 volts is treated as a high logic level, an IC output signal under 0.5 volts is treated as a low logic level, and an IC output signal between 0.5 and 4.5 volts is considered neither high nor low logic level. Thus comparators 38 and 39 and DACs 40 and 41 can be thought of as an analog-to-digital converter (ADC) producing a 2-bit thermometer code output {CH, CL} indicating one of three ranges in which the input signal voltage lies.

Data acquisition circuit 30 samples the CH and CL bits at a time during each test cycle when the IC output signal is expected to be at a particular logic level. If the IC output signal is expected to be at its high logic level, then the CH bit should be true and the CL bit should be false when sampled. If the IC output signal is expected to be at is low logic level then CL should be true and CH should be false when sampled. An IC under test is considered to be defective when the sampled CH and CL bits representing the state of any of the IC's output signals are not of their expected states during any test cycle.

In some testers data acquisition and control circuit 30 stores the CH and CL bit for each test cycle in an acquisition memory so that a host computer can access the data via bus 42 at the end of the test and determine whether the IC is defective. In other testers circuit 30 may compare the

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sampled CH and CL data produced during each test cycle to their expected values and store cycle numbers in an internal memory referencing the particular test cycles, if any, for which the sampled data fails to match their expected values. The host computer then accesses the stored cycle numbers via bus **42**.

While tester channels **24** in some testers include two comparators as illustrated in FIG. **3**, tester channels in other testers may include only a single comparator. For example when the low and high logic levels of an IC output signal are 0 and 5 volts, respectively, the comparator may be set to drive its single-bit output signal true when the IC output signal exceeds 2.5 volts. Also in many testers channel do not include their own DACs; centralized DACs provide reference voltages in common to all channels.

One drawback to the test system illustrated in FIGS. **2** and **3** is that it requires one tester channel **24** for every pad **26** on wafer **14**. Since a wafer **14** can have a large number of ICs **12**, and since each IC may have a large number of such pads **26**, tester **10** would require a very large number of channels in order to concurrently access all pads **26** of all ICs **12**.

What is needed is a system permitting a tester having a limited number of tester channels to concurrently test ICs having a larger number of input and output pads.

BRIEF SUMMARY OF THE INVENTION

Integrated circuits (ICs) formed on a semiconductor typically include conductive pads on their surfaces for receiving IC input signals and for transmitting IC output signals. The invention relates in general to a system for testing ICs before the wafer is cut to separate them, and in particular to an interconnect system for linking a single IC tester channel to multiple (N) IC input or output pads in a way that allows the tester channel to either concurrently transmit a test signal to all N IC input pads or to concurrently monitor and determine states of output signals produced at all N IC output pads.

An interconnect system in accordance with an exemplary embodiment of the invention may include a probe card providing signal paths between the various channels of an IC tester and probes accessing the input and output pads on the surface of the ICs. When a single tester channel is to be connected to each of N IC pads, the probe card provides a branching signal path for distributing the test signal produced by the tester channel to probes accessing each of the N IC pads. Each branch of the path includes a resistor for isolating the IC input pad accessed via that branch from all other branches of the path so that a fault on the IC input pad accessed via that branch does not substantially affect the voltage of the test signal passing through any other branch.

When a single tester channel is to transmit a test signal to all N IC pads, but is not to monitor IC output signals produced at any N IC pads, the resistance of the resistors included in all path branches may be of similar size. However when a single tester channel is to monitor IC output signals produced at all N IC pads, each branch includes a uniquely sized scaling resistor so that each of the 2^N combinations of logic states of the signals produced at the N IC output pads results in a different tester channel input signal voltage. In such case, the tester channel measures the voltage of its input signal and the logic state of each of the signals produced at each of the N IC output pads is determined from the measured voltage of the input signal.

The claims appended to this specification particularly point out and distinctly claim the subject matter of the invention. However those skilled in the art will best understand both the organization and method of operation of what

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the applicant considers to be the best modes of practicing the invention, together with further advantages and objects of the invention, by reading the remaining portions of the specification in view of the accompanying drawings wherein like reference characters refer to like elements.

BRIEF DESCRIPTION OF THE DRAWING(S)

FIG. **1** is a plan view of a prior art semiconductor wafer upon which integrated circuits (ICs) are formed,

FIG. **2** is a simplified side elevation view of a prior art wafer level IC test system,

FIG. **3** is a block diagram illustrating a portion of the prior art wafer level IC test system of FIG. **3**,

FIG. **4** is a simplified side elevation view of a wafer level IC test system in accordance with an exemplary embodiment of the invention,

FIG. **5** is a block diagram of the wafer level IC test system of FIG. **4**,

FIG. **6** is a schematic and block diagram of a portion of the wafer level test system of FIG. **5**,

FIGS. **7–11** are schematic diagrams illustrating a portion of the wafer level test system of FIG. **5**,

FIGS. **12–14** illustrate alternative embodiments of the analog-to-digital converter of FIG. **6**,

FIG. **15** is a side elevation view of a probe assembly in accordance with an exemplary embodiment of the invention for providing signal paths between an integrated circuit tester to and a wafer, and

FIGS. **16–19** are schematic diagrams illustrating alternative versions of the signal paths provided by the probe assembly of FIG. **15**.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS OF THE INVENTION

This specification describes one or more exemplary embodiments and/or applications of an invention considered by the applicant(s) to be the best modes of practicing the invention. However those of skill in the art will appreciate that there are other modes of practicing the invention, and there is no intention that the invention be limited to the particular embodiment(s) described below or to the manner in which the embodiments operate. The scope of the invention is defined by the claims appended to this specification.

The present invention relates to an apparatus for providing signal paths between an IC tester and terminals of ICs through which the ICs transmit and receive signals so that the tester can test the ICs. Some testers can test many ICs concurrently while they are still in the form of unseparated die on a semiconductor wafer. ICs typically include conductive pads on their surfaces that can act as terminals for receiving IC input signals from external circuits and for transmitting IC output signals to external circuits. While an interconnect system in accordance with an exemplary embodiment of the invention described herein below connects an IC tester to pads of ICs while still in the form of die on a semiconductor wafer, it should be understood that the invention could be employed to connect IC testers to pads of separated unpackaged ICs or to pins or other types of terminals of packaged ICs may also be adapted to employ the invention as described herein below.

FIGS. **4** and **5** illustrate an exemplary system **50** for testing a set of ICs **52** formed on a semiconductor wafer **54**. A set of coaxial cables **56** couple each channel **57** of an IC tester **58** to a connector **60** on the upper surface of a probe

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card 62. Probe card 62 provides signal paths linking the ends of conductors 56 at connector 60 to a set of probes 64. Any type of probe card may be employed. Non-exclusive examples include a single printed circuit board (PCB) with probes attached directly to the PCB (as employed in exemplary system 50) and probe card assemblies including several separate substrate layers interconnected by spring contacts or other means. Other non-exclusive examples of probe cards are disclosed in U.S. Pat. No. 5,974,662 issued Nov., 2, 1999 to Eldridge et al., and U.S. Pat. No. 6,064,213 issued May 16, 2000 to Khandros et al., each of which is incorporated herein by reference.

Various types of structures can be used to implement probes 64 including, for example, wire bond and lithographic spring contacts, needle probes, and cobra probes. When spring contacts are employed to implement probes 64, they can be attached to pads formed on a lower side of probe card 62 and arranged so that their downward extending tips contact a set of pads 71 and 72 formed on the surfaces of ICs 52. Spring contact probes 64 may alternatively be formed on pads 71 and 72 with tips of probes 64 extending upward to contact the pads formed on the lower surface of probe card 62. Pads 71 and 72 may be the ICs' input/output (I/O) terminals or may be redistribution pads that are linked to the ICs' I/O terminals.

U.S. Pat. No. 6,064,213, issued May 16, 2000 to Khandros et al. (incorporated herein by reference) discloses an example of a card assembly designed to contact spring contacts formed on an IC. U.S. patent application Ser. No. 09/810,871 filed Mar. 16, 2001 (incorporated herein by reference) describes another example of a card assembly employing spring contact probes. U.S. Pat. No. 5,974,662 issued Nov. 2, 1999, issued to Eldridge et al., incorporated herein by reference, describes an example of a probe card assembly in which spring contacts formed on a probe card function as probes. The following documents (incorporated herein by reference) disclose various exemplary methods for manufacturing spring contacts: U.S. Pat. No. 6,333,269 issued Jan. 8, 2002 to Eldridge et al., U.S. Pat. No. 6,255,126 issued Jul. 31, 2001 to Mathieu et al., U.S. patent application Ser. No. 09/710,539 filed Nov. 9, 2000, and U.S. patent application Ser. No. 09/746,716 filed Dec. 22, 2000.

Tester 58 typically organizes a test into a succession of test cycles of uniform duration, and during each test cycle each tester channel 57 may generate an output test signal to be supplied to one or more of IC pads 71 and 72 or may receive an input signal having a voltage representing a logic state of IC output signals generated at pads 71 and 72. Before starting a test, a host computer 63 supplies programming instructions to channels 57 via a bus 65 telling each channel 57 what to do during each test cycle.

Some of the pads 71 on the surface of a wafer 54 may act as IC input terminals that can only receive IC input signals generated by channels 57. For example, the pads linked to control and address terminals of a RAM or of a read only memory (ROM) are uni-directional input terminals.

Other pads 72 on wafer 54 may act as uni-directional IC output terminals that can only produce IC output signals at the pads or as bi-directional input/output terminals that can both transmit and receive signals. For example, pads linked to data terminals of a ROM are uni-directional output pads whereas the pads linked to data terminals of a RAM are bi-directional I/O pads.

If tester 58 were to include a separate tester channel 57 for each pad 71 or 72, probe card 62 could provide a separate signal path 68 between each pad 71 or 72 and its corre-

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sponding tester channel 57. For example ICs 52 might be RAMs for storing 8-bit data at 8-bit addresses. The RAMs could be tested by writing data to each address and then reading the data back out to determine whether it matches the data written into that address. Each RAM would have eight input pads 71 for receiving an address, eight I/O pads 72 for transmitting and receiving data, and, for example, two input pads 71 for receiving control signals. If probe card 62 were to connect only one pad to each channel 57, IC tester 58 would have to provide 18 channels 57 for each RAM to be tested. If wafer 54 contained 100 RAMS, then tester 58 would have to have 1800 channels in order to test all RAMs concurrently.

Since all ICs 52 formed on wafer 54 are usually similar and are tested in the same way and at the same time, each IC 52 would receive the same set of input address and control signals during any given test cycle. To reduce the number of tester channels 57 needed, probe card 62 provides a set of branching signal paths 74, each for linking one tester channel 57 to more than one IC input pad 71. For example, when the ICs 52 being tested are RAMs having 8-bit input addresses A0–A7, probe card 62 delivers an output signal of one tester channel 57 as the A0 address input to each of multiple (N) RAMs, seven other tester channels 57 supply the A1–A7 address bits to the same set of N RAMs. Thus only eight channels 57, rather than 8*N channels, are needed to supply an 8-bit address to each of N RAMs. Similarly branched paths 74 may be provided to deliver a control signal produced by one channel 57 to inputs pads of N RAMs.

Various faults can occur at any input pad 71. For example a pad 71 may be shorted through a low impedance path to ground, to a power source, or to a nearby signal pad 71 or 72. Each branch of a signal path 74 delivering an input signal to more than one IC input pad 71 includes an isolation resistor 75. All resistors 75 in paths 74 linked to uni-directional input pads 71 may be of similar or differing resistance, however all isolation resistors 75 are of sufficient size that a fault at any one IC input pad 71 will not substantially influence the voltage of the channel output signal VOUT supplied to any other IC input pad 71 through the same path 74.

Probe card 62 also provides another set of branching signal paths 76, each linking a set of N IC output or I/O pads 72 to the same circuit node 84 within the probe card. When pads 72 are to receive input signals, a single tester channel 57 supplies the same input signal to all N pads 72 via the branching path 76. When pads 72 are to produce output signals, a signal developed at node 84 of path 76 in response to the N IC output signals produced at pads 72 is supplied as an input signal to a single tester channel 57.

Each ith branch of an N-branch signal path 76 includes a scaling resistor 77 of magnitude R_i. The scaling resistors 77 in the branches of any signal path 76 are all of differing resistances so that the voltage of the signal developed at node 84 depends on the combination of logic states of all of the IC output signals produced at the N output pads 72 linked to node 84. Assuming the N IC output signals form an N-bit binary number, then with values of resistors 77 appropriately chosen, the voltage of the signal developed at node 84 will be a monotonic function of the value of that binary number. When a tester channel 57 measures the voltage of the signal developed at one of nodes 84 with sufficient resolution, it is possible to determine the logic state of each of the N signal produced at the IC output pads 72 that are linked to that node.

FIG. 6 shows a set of N drivers 80 within ICs formed on wafer 54 generating a set of N output signals V_1–V_N

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produced at IC output pads **72**. Probes **64** deliver output signals V_1–V_N to a set of pads **82** on the lower surface of probe card **62**. Probe card **62** provides a branching path **76** including scaling resistors R_1–R_N for linking pads **82** to a common node **84**. A coaxial cable **56** links node **84** to an input terminal **86** of a tester channel **57**. When coaxial cable **56** has a characteristic impedance of, for example 50 Ohms, an optional 50 Ohm resistor RIN may be provided within tester channel **57** to terminate the coaxial cable when necessary to eliminate signal reflections at terminal **86**. Termination resistor RIN may not be needed in applications where such signal reflections are not problematic.

Tester channel **57** includes an analog-to-digital converter (ADC) **88** for receiving the VIN signal and for producing M-bit thermometer code output data (DATA). Each of the M+1 possible values of DATA represents a different voltage range. The current value of DATA indicates the particular range within which the voltage of the ADC's VIN input signal resides. Each tester channel **57** also includes a data acquisition and control circuit **90** supplying reference data DREF as input to ADC **88** for controlling the relationship between each value of DATA and the voltage range it represents.

Circuit **90** also samples the value of the DATA output of ADC **88** at a time during each test cycle at which the V_1–V_N signals are expected to stabilize at their expected logic levels. Before starting a test, host computer **63** of FIG. 5 programs circuit **90** with instructions supplied via bus **66** telling it how to adjust the range of ADC **88** and indicating times during each test cycle at which the DATA value is to be sampled. In one embodiment of the invention, circuit **90** stores the sampled value of DATA for each test cycle so that host computer **63** (FIG. 5) can thereafter read the sampled DATA value to determine the voltage of the VIN signal produced during each cycle of the test. This enables the host computer to determine the logic state of each IC output signal V_1–V_N during each test cycle. Alternatively, the instructions that the host computer supplies to control circuit **90** before the start of the test may indicate expected values of the DATA output of ADC **88** for each test cycle. Circuit **90** then determines from DATA value acquired during each test cycle whether any output signal V_1–V_N is of an incorrect state during any test cycle.

Assume, for example, that N=2, so that probe card **62** links two IC output pads **72** to the input **86** of one tester channel **57**. Assume also that the nominal low and high logic levels for each output signal V_1–V_N are 0 and 5 volts, the output impedance of each driver **80** is much lower than 50 Ohms, and the input impedance of ADC **88** is much higher than 50 Ohms. Further, assume as depicted in FIGS. 7–10 that RIN=50 Ohms, R_1=50 Ohms, and R_2=25 Ohms. Then as illustrated in FIG. 7, when both V_1 and V_2 are 0 volts, VIN will be 0 volts. As illustrated in FIG. 8, when both V_1 and V_2 are 5 volts, VIN will be 3 volts. FIG. 9 shows that when V_1 is 0 volts and V_2 is 5 volts, VIN will be 2.5 volts. As seen in FIG. 10, when V_1 is 5 volts and V_2 is 0 volts, VIN will be 2 volts. Table I summarizes the relationships between voltage magnitudes of V_1, V_2 and VIN.

TABLE I

V_2	V_1	VIN
0	0	0
0	5	2
5	0	2.5

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TABLE I-continued

V_2	V_1	VIN
5	5	3

Since VIN may be of any of four different voltage levels depending on the logic states of the V_1 and V_2 signals, it is possible to determine the logic state of each signal when ADC **88** is able measure the voltage of VIN with sufficient resolution. When M=3, ADC **88** produces a 3-bit output thermometer code DATA which can represent any of four voltage ranges. In such case circuit **90** may, for example, set the DREF data input to ADC **88** so that ADC **88** responds to values of VIN in the ranges indicated in TABLE II by producing the indicated values of the 3-bit thermometer code DATA.

TABLE II

VIN	DATA
VIN < 1.75	000
1.75 V < VIN < 2.25 V	001
2.25 V < VIN < 2.75 V	011
2.75 V < VIN	111

With these ADC settings, the data input to data acquisition and control circuit **90** distinguishes from among the four possible voltage levels of the VIN signal and therefore enables circuit **90** or the host computer to determine the logic state each of the IC output signals V_1 and V_2 from which the VIN signal is derived.

FIG. 11 illustrates an example in which N=3 such that probe card **62** of FIG. 6 links the output pads **72** of three ICs **52** to the input terminal of a single tester channel **57**. Assume again that the low and high logic levels of the IC output signals V_1–V_3 produced at the three IC output pads **72** are 0 and 5 volts and that the input impedance of ADC **88** is very high, and the output impedance of drivers **80** is very low. In this example we assume signal reflections at terminal **86** of channel **57** are not problematic and that no resistor RIN is needed to terminate coaxial cable **56** with its characteristic impedance.

As illustrated in FIG. 11 we can, for example, set R_1=100 Ohm, R_2=50 Ohms and R_3=25 Ohms. Table III below illustrates the possible combinations of V_1–V_3 voltages and the VIN voltage resulting from each combination:

TABLE III

V_3	V_2	V_1	VIN
0	0	0	0
0	0	5	0.71
0	5	0	1.43
0	5	5	2.14
5	0	0	2.86
5	0	5	3.57
5	5	0	4.29
5	5	5	5

When ADC **88** is capable of producing a 7-bit output thermometer code DATA, circuit **90** may, for example, set ADC **88** to respond to values of VIN in the ranges indicated in TABLE IV below by producing the indicated values of thermometer code DATA.

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TABLE IV

VIN	DATA
VIN < .35 V	0000000
.35 v < VIN < 1.05 V	0000001
1.05 V < VIN < 1.75 V	0000011
1.75 V < VIN < 2.50 V	0000111
2.50 V < VIN < 3.20 V	0001111
3.20 V < VIN < 3.90 V	0011111
3.90 V < VIN < 4.65 V	0111111
4.65 V < VIN	1111111

In general, when probe card 62 employs a set of N scaling resistors R_1–R_N of appropriately dissimilar resistances to combine the output signals V_1–V_N of a set of N IC output pads 72 to form a single signal input VIN to ADC 88, the various combinations of V_1–V_N logic states may drive the VIN signal to any of 2^N voltage levels. In order to enable data acquisition and control circuit 90 or a host computer to distinguish from among the 2^N VIN possible voltage levels, and therefore to determine the logic state of each signal V_1–V_N, the DATA output of ADC 88 is preferably at least $M=2^N-1$ bits wide, and the voltage ranges represented by each value of DATA must be appropriately selected.

However as illustrated in FIG. 3, a channel 24 of a prior art IC tester to be employed in this application may have, for example, only two comparators 38 and 39. Such a tester channel 24 can compare a VIN signal to only two reference levels VH and VL produced by a pair of digital-to-analog converts (DACs) 40 and 41. Thus comparators 38 and 39 and DACs 40 and 41 can act as an ADC capable of producing only a 2-bit thermometer code {CH, CL} representing the voltage level of the VIN signal as residing within one of only three ranges. Tester channels in some prior art IC testers include only a single comparator acting as a single-bit ADC that can distinguish between only two voltage ranges.

When a probe card in accordance with an exemplary embodiment of the invention combines multiple (N) IC output signals in the manner described above to produce a VIN signal input to a tester channel having only one or two comparators, the channel's 1 or 2 bit comparator output does not represent the voltage of the VIN signal with sufficient resolution to enable a host computer to determine the state of each of the N IC output signal V_1–V_N. Nonetheless, it is possible to use a conventional tester channel producing only a 1-bit or 2-bit thermometer code output (i.e. M<3) to monitor a VIN signal representing multiple IC output signals V_1–V_N, and yet provide sufficient information to enable the host computer to determine the state of all signals V_1–V_N during each test cycle.

One way to do that is perform the same test on the ICs several times, with the comparator reference voltages being set to different values during each repetition of the test. For example, assume that three IC output signals V_1–V_3 having low and high states of 0 volt and 5 volts are combined as illustrated in FIG. 11 to provide a single VIN input to a tester channel having only a single comparator. Thus, referring to FIG. 6, N is 3 and M is 1. VIN could be of any of 8 levels as illustrated in Table III above. Since the ADC output DATA has only a single bit and can only represent two VIN voltage ranges and not eight, data acquisition and control circuit 90 is programmed to run the test seven times. For example, referring to Table IV above, during all cycles of the first repetition of the test, ADC 88 is set to drive the single-bit DATA to a 1 when VIN exceeds 0.35 volts. During all cycles of the second repetition of the test, ADC is set to

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drive DATA to a 1 only when VIN exceeds 1.05 volts. During the third through the seventh repetitions of the test, ADC is set to drive DATA to a 1 when VIN exceeds 1.05V, 1.75V, 2.50V, 3.20 v, 3.90V, and 4.65V, respectively. The seven bits of data acquired during the Kth cycle of each of the seven repetitions of the test will enable the host computer 63 to determine the state of each signal V_1–V_3 during that Kth test cycle.

When data acquisition and control circuit 90 is capable of adjusting the DREF input to ADC 88 at the start of each test cycle (rather than only at the start of each test), test cycles in which the IC's output signals states are to be determined can be repeated 7 times using a different value of DREF for each repetition. For example when a single tester channel is monitoring data bit outputs V_1–V_3 of a ROM IC, the ROM's address inputs are kept the same for seven test cycles so that each ROM continues to read out data at the same address for seven test cycles. However DREF is set to a different value for each of the seven cycles so that the state of each bit V_1–V_3 can be determined from the sequence of seven DATA bits produced during those seven test cycle.

Increasing the number M of bits in the DATA output of ADC 88 decreases the number of times each data read cycle must be repeated in order to gather a sufficient amount of data to determine the voltage level of each of the combined IC output signals. For example a tester channel having two comparators acting as an ADC 88 producing a 2-bit (M=2) output DATA could be used to monitor a VIN signal representing the combination of three IC output signals V_1–V_3 if each test cycle were repeated four times, with the DREF data being appropriately adjusted prior to each test repetition.

The M-bit ADC 88 of FIG. 6 may have any of a variety of architectures. FIG. 12 illustrates an exemplary ADC having M comparator units 94(1)–94(M), each including a comparator 95 and a DAC 96. The DAC 96 of each comparator unit 94 converts a separate field of the DREF data into a reference voltage VREF. The comparator 95 of each unit 94 compares the VIN signal to reference voltage VREF to produce a separate bit of M-bit output DATA.

FIG. 13 illustrates another suitable architecture for ADC 88 of FIG. 6. Selected values of the DREF data are written into successive addresses of a RAM 100 addressed by the output ADDR of a counter 102. A DAC 104 converts data read out of RAM 100 into a reference voltage VREF supplied as input to a comparator 106 which compares VREF to VIN and asserts its output COMP when VREF is higher in voltage than VIN. A leading edge of the COMP output of comparator 106 clocks a register 108 which stores the ADDR output of counter 102. Register 108 supplies its contents as the ADC's DATA output. A START signal pulse supplied by circuit 90 of FIG. 6 marks a point during each test cycle at which the VIN data is expected to stabilize to a high or logic level. The START signal resets the counter's ADDR output to 0, and thereafter counter 102 increments its ADDR output on each pulse of a clock signal CLK so that RAM 100 successively reads out DREF data stored at successive RAM addresses. DAC 104 responds to the continuously increasing DREF data by continuously increasing the VREF input to comparator 106. When VREF exceeds VIN, comparator 106 asserts the COMP signal causing register 108 to store the current ADDR output of counter 102. Thus by the time counter 102 has reached its count limit during the test cycle, register 108 will have stored the ADDR value resulting in the lowest VREF voltage that exceeds VIN. In this version of ADC 88, the DATA value can appear in binary-encoded form rather than in thermometer code

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form. With the DREF data stored in RAM **100** providing a sufficient number of appropriately adjusted VREF levels, a host computer can determine the V_1–V_N signal states from the DATA output of register **108**.

FIG. **14** illustrates a version of ADC **88** of FIG. 6 suitable for use in a tester that is customized to test a particular kind of IC. In such case, the reference voltage levels represented by the various values of DATA need not be adjustable. The ADC of FIG. **14** includes a resistor network **110** dividing a supply voltage VDD to produce a set of reference voltages VREF(1)–VREF(M) supplied as input to a set of M comparators **112**(1)–**112**(M). Each comparator **112** compares its input reference voltage to VIN to produce a separate bit of the ADC's output DATA.

FIG. **15** illustrates another exemplary embodiment of the invention, a multiple-layer probe card assembly **120** for providing signal paths between an integrated circuit tester **122** and pads **123** on surfaces of IC dice **124** on a wafer **126** under test. Probe card assembly **120** includes a probe board **130** having a set of pads **132** on its upper surface for receiving tips of a set of pogo pin connectors **134** providing signal paths between tester **122** and pads **132**. An interposer layer **135** having a set of spring contacts **136** and **138** connected to its upper and lower surfaces provides signal paths between a set of contacts **140** on the lower surface of probe board **130** and a set of contacts **142** on an upper surface of a space transformer board **144**. A set of probes **146** provide signal paths between pads **148** on the lower surface of space transformer **144** and IC pads **123**. Probe board **130**, interposer **138** and space transformer **144** may include single or multiple insulating substrates with traces formed on the substrates and vias extending through the substrate for conducting signals horizontally and vertically between pads and/or contacts on their upper and lower surfaces.

In accordance with this exemplary embodiment of the invention, some of the signal paths though probe board assembly **120** branch so that a channel of IC tester **122** employing a single one of pogo pins **134** as an input and/or output terminal can concurrently access more than one IC pad **123**. Isolation resistors (not shown in FIG. **15**) formed on or within one or more of layers **130**, **135** and **144** are included in the branching paths between pogo pins **134** and IC pads **123**.

FIGS. **16**–**19** are schematic diagrams illustrating various alternative versions of a branching signal path within probe board assembly **120**. In FIG. **16** the isolation resistors **150** are formed on or between layers of probe board **130**. In the versions of FIGS. **17** and **18**, the isolation resistors **150** are formed on or between layers of interposer **135** and space transformer **134**. A hierarchical resistor network may also be implemented by mounting resistors on one or more boards of probe board assembly **120**. For example, FIG. **19** illustrates a signal path including a hierarchy of isolation resistors **150** formed on probe board **130** and on space transformer **134**. Resistors **150** may be of suitably differing values as described above when one tester channel is to monitor IC output signals at more than one IC pad **123**.

Thus has been shown and described a probe card for providing signal paths between IC tester channels and input and output pads the surfaces of ICs formed on a semiconductor wafer wherein some of the paths link one tester channel to more than one input or output pad. The forgoing specification and the drawings depict the best modes of practicing the invention, and elements or steps of the depicted best modes exemplify the elements or steps of the invention as recited in the appended claims. However the appended claims are intended to apply to any mode of

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practicing the invention comprising the combination of elements or steps as described in any one of the claims, including elements or steps that are functional equivalents of the example elements or steps depicted in the specification and drawings.

What is claimed is:

1. An apparatus for providing signal paths between integrated circuit (IC) tester channels and input and output pads residing on surfaces of a plurality of ICs, wherein the ICs are adapted to receive test signals via the input pads and to generate output signals at the output pads in response to the test signals, and wherein voltages of the test signals and the output signals represent logic states, the apparatus comprising:

a first node; and

N first signal paths,

wherein N is an integer greater than one,

wherein each first signal path links a separate one of the output pads to the first node, such that a first signal is produced at the first node in response to a set of N output signals generated at the output pads linked to the first node, and

wherein all N first signal paths have substantially differing resistances such that a voltage of the first signal has a unique magnitude for each unique combination of logic states of the set of N output signals.

2. The apparatus in accordance with claim 1 further comprising first conductive means for delivering the first signal appearing at the first node as an input signal to one of the IC tester channels.

3. The apparatus in accordance with claim 1 further comprising:

a second circuit node;

a plurality of second signal paths, each corresponding to a separate one of the IC input pads and delivering a test signal from the second circuit node to the corresponding IC input pad, wherein each second signal path is of sufficient resistance that a short linking the corresponding IC input pad to any source of potential within the IC upon which the IC input pad resides would not alter the logic state of the test signal at the second circuit node.

4. The apparatus in accordance with claim 3 further comprising:

first conductive means for delivering the first signal appearing at the first node as an input signal to one of the IC tester channels, and

second conductive means for delivering a test signal produced by another of said tester channels to the second circuit node.

5. An apparatus for providing signal paths between integrated circuit (IC) tester channels and input pads and output pads residing on surfaces of a plurality of ICs, wherein the ICs are adapted to receive test signals via the input pads and to generate output signals at the output pads in response to the test signals, and wherein voltages of the test signals and the output signals represent logic states, the apparatus comprising:

at least one substrate having a surface;

a first circuit node formed on said at least one substrate;

N first conductive pads formed on said surface, where N is an integer greater than 1;

N first probes, each first probe linking a separate one of N of said output pads to a corresponding one of the N first conductive pads; and

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N first signal paths, each linking a corresponding one of the N first conductive pads to said first circuit node such that a first signal is produced at the first circuit node in response to a set of N output signals generated at the output pads linked to the first circuit node, all N first signal paths have substantially differing resistances such that a voltage of the first signal has a unique magnitude for each unique combination of logic states of the set of N output signals.

6. The apparatus in accordance with claim 5 wherein portions of the N first signal paths are formed on said at least one substrate.

7. The apparatus in accordance with claim 5 wherein said at least one substrate comprises:

a first substrate having said surface; and

a second substrate, spaced from said first substrate, said first circuit node being formed on said second substrate, wherein said first signal paths are formed on and extend between the first and second substrates.

8. The apparatus in accordance with claim 5 where said at least one substrate comprises:

a first substrate having said surface; and

a second substrate, spaced from said first substrate, said first circuit node being formed on said second substrate; and

a third substrate residing between and spaced from said first and second substrates, wherein said first signal paths are formed on and extend between the first, second and third substrates.

9. The apparatus in accordance with claim 5 further comprising first conductive means for delivering the first signal appearing at the first circuit node as an input signal to one of the IC tester channels.

10. The apparatus in accordance with claim 5 wherein each first probe comprises a spring contact.

11. The apparatus in accordance with claim 5 wherein the apparatus further comprises:

a second circuit node formed on the substrate;

a plurality of second conductive pads formed on the surface of the substrate;

a plurality of second probes, each second probe linking a separate one said input pads to a corresponding one of the plurality of second conductive pads; and

a plurality of second signal paths, each corresponding to a separate one of the second conductive pads for delivering a test signal applied to the second circuit node to the corresponding second conductive contact, wherein each second signal path has substantial resistance sufficient to prevent a fault at any of the inputs pads from affecting a logic state of the test signal applied at the second circuit node.

12. The apparatus in accordance with claim 11 further comprising:

first conductive means for delivering the first signal appearing at the first circuit node as an input signal to one of the IC tester channels, and

second conductive means for delivering a test signal produced by another of said tester channels to the second circuit node.

13. The apparatus in accordance with claim 12 wherein each first probe and each second probe comprises a spring contact.

14. An apparatus for testing integrated circuit (ICs), wherein the ICs have input pads at which the ICs receive test signals, and have output pads at which they produce output

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signals in response to the test signals, the test and output signals having voltages representing logic states, the apparatus comprising:

a first circuit node;

N first signal paths, wherein N is an integer greater than one, wherein each first signal path links a separate one of the output pads to the first circuit node, and wherein each first signal path has a resistance differing substantially from a resistance of any other of the first signal paths, such that a first signal appears at the first circuit node having a first voltage representing a combination of logic states of the output signals produced by the output pads linked by the first signal paths to the first circuit node; and

a first IC tester channel linked to the first circuit node including means for measuring the first voltage of the first signal.

15. The apparatus in accordance with claim 14 wherein the means for measuring the first voltage of the first signal comprises an analog-to-digital converter (ADC) for generating output data in response to the first signal, wherein a value of the output data represents a voltage range in which said first voltage resides.

16. The apparatus in accordance with claim 15 wherein the ADC comprises:

a digital-to-analog converter (DAC) for generating a reference voltage of magnitude determined by a value of control data supplied as input to the DAC; and

a comparator receiving the reference voltage and the first signal for generating an output bit indicating whether the first voltage is greater than the reference voltage.

17. The apparatus in accordance with claim 16 wherein the ADC further comprises means for periodically altering the value of the control data.

18. The apparatus in accordance with claim 15 wherein the ADC comprises:

means for generating M reference voltages, of substantially differing magnitudes, where M is an integer greater than 1, and

M comparators, each comparator corresponding to a separate one of the M reference voltages, each comparator receiving its corresponding reference voltage and the first signal as inputs, and each comparator generating a separate bit of an M-bit data word, wherein the bit generated by each comparator indicates whether the first voltage is greater than its corresponding reference voltage.

19. The apparatus in accordance with claim 18 wherein M is at least as large as 2^N-1 and wherein the magnitudes of said M reference voltages are such that each possible combination of logic states of the output signals produced by the output pads linked by the first signal paths to the first circuit node results in a unique value of the M-bit data word.

20. A method for testing at least one integrated circuit (IC) device wherein at least one IC device comprises a plurality of terminals at which said at least one IC device receives input signals and concurrently produces output signals, wherein voltages of the input and output signals represent logic states, the method comprising the steps of:

a. providing a first circuit node;

b. providing a plurality of first signal paths, each first signal path linking a separate one of the plurality of terminals to the first circuit node, such that a first signal is produced at the first circuit node in response to IC output signals concurrently generated at each of the plurality of IC terminals, wherein all first signal paths

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have substantially differing resistances such that a voltage of the first signal produced at the first circuit node has a unique magnitude for each unique combination of logic states of the IC output signals produced at the plurality of IC terminals;

c. measuring a voltage of the first signal produced at the first circuit node; and

d. determining a logic state of each of the plurality of output signals from the voltage measured at step c.

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21. The method in accordance with claim 20 further comprising the step of:

e. applying a test signal to the first circuit node such that the test signal travels from the first circuit node to each of the plurality of IC terminals via a separate one of the first signal paths, such that the test signal becomes an input signal received by each of the plurality of IC terminals.

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Roy et al.   (45) **Date of Patent:**   **Jan. 13, 2004**

(54) **DISTRIBUTED INTERFACE FOR PARALLEL TESTING OF MULTIPLE DEVICES USING A SINGLE TESTER CHANNEL**

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(52) **U.S. Cl.** **714/730**; 714/719
(58) **Field of Search** 714/724, 730, 714/718, 719

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(57) **ABSTRACT**

A system for testing a number of integrated circuit (IC) devices under test (DUTs) having interface circuitry coupled to a single or multi-channel tester for receiving data values from the tester and providing error information concerning the DUTs. The interface circuitry forwards data values (received from the tester over a single channel) to a number of DUTs in parallel. The circuitry performs comparisons using data values read from the DUTs, and in response generates error values indicative of the comparison. The error values may then be returned to the tester over the same or a different channel.

20 Claims, 11 Drawing Sheets
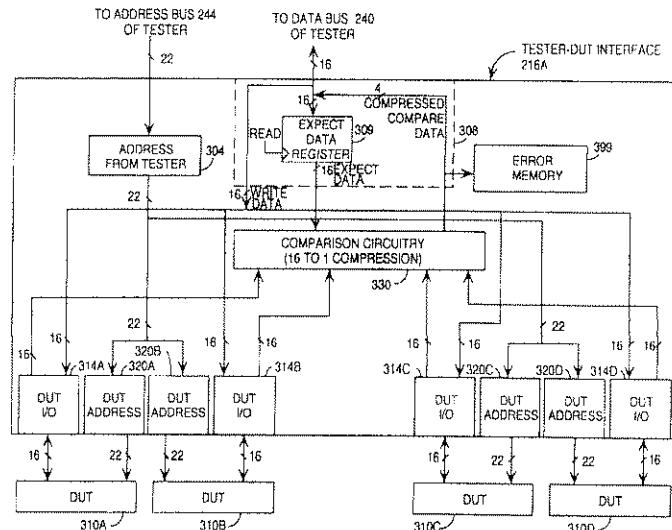
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Fig. 1
(Prior Art)

Fig. 2

Fig. 3

Fig. 4

(START)

GENERATE TEST SEQUENCE ADDRESSES AND DATA BY TESTER AS INPUTS TO A DUT, ADCCORDING TO CONVENTIONAL TECHNIQUES   504

TESTER SENDS ADDRESS AND DATA ON MULTIPLE TESTER CHANNELS SIMULTANEOUSLY, ACCORDING TO CONVENTIONAL TECHNIQUES   508

INTERFACE CIRCUITRY RECEIVES ADDRESS AND DATA FROM A SINGLE CHANNEL AND APPLIES TO A NUMBER OF DUTS SIMULTANEOUSLY   512

TESTER RUNS REFRESH CYCLES (IF DUTs ARE MEMORY DEVICES), LONG CYCLE TESTS, AND OTHER TEST PATTERNS ON MULTIPLE TESTER CHANNELS, ACCORDING TO CONVENTIONAL TECHNIQUES   516

INTERFACE CHIP APPLIES THE DATA OF SOME OR ALL OF THE TESTS IN STEP 516 TO ALL DUTSs   518

TESTER SENDS THE EXPECTED DATA ON MULTIPLE TESTER CHANNELS, ACCORDING TO CONVENTIONAL TECHNIQUES   519

INTERFACE CHIP READS DATA FROM DUTs AND PERFORMS COMPARISONS WITH EXPECTED DATA TO DETERMINE IF THERE ARE ANY ERRORS IN THE READ DATA; APPROPRIATE ERROR STORAGE AND COMPRESSION TAKES PLACE   520

TESTER REQUESTS ERROR DATA ON MULTIPLE TESTER CHANNELS SIMULTANEOUSLY, REQUESTING ERROR DATA THAT WAS PRODUCED IN STEP 520   524

INTERFACE CHIP RESPONDS BY PROVIDING NEW ERROR INFORMATION CONCERNING EACH OF THE DUTs   528

TESTER RECONGINZES THE NEW ERROR INFORMATION, UPDATES THE STORED ERROR INFORMATION FOR EACH OF THE DUTs   532

Fig. 5

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              ┌──────────┐
              │  START   │
              └──────────┘
                   │
                   ▼
  ┌────────────────────────────────────────────────────────┐
  │ GENERATE TEST SEQUENCE ADDRESSES AND DATA BY TESTER AS  │
  │ INPUTS TO A DUT, ADCCORDING TO CONVENTIONAL TECHNIQUES  │
  │                                                    604   │
  └────────────────────────────────────────────────────────┘
                   │
                   ▼
  ┌────────────────────────────────────────────────────────┐
  │ TESTER SENDS ADDRESS AND DATA ON MULTIPLE TESTER        │
  │ CHANNELS SIMULTANEOUSLY, ACCORDING TO CONVENTIONAL      │
  │ TECHNIQUES                                         608   │
  └────────────────────────────────────────────────────────┘
                   │
                   ▼
  ┌────────────────────────────────────────────────────────┐
  │ RECEIVE ADDRESS AND DATA FROM A SINGLE CHANNEL AND      │
  │ APPLY TO A NUMBER OF DUTS SIMULTANEOUSLY BY AN          │
  │ INTERFACE CHIP                                     612   │
  └────────────────────────────────────────────────────────┘
                   │
                   ▼
  ┌────────────────────────────────────────────────────────┐
  │ TESTER RUNS REFRESH CYCLES (IF DUTs ARE MEMORY          │
  │ DEVICES), LONG CYCLE TESTS, AND OTHER TEST PATTERNS ON  │
  │ MULTIPLE TESTER CHANNELS, ACCORDING TO                 │
  │ CONVENTIONAL TECHNIQUES                            616   │
  └────────────────────────────────────────────────────────┘
                   │
                   ▼
  ┌────────────────────────────────────────────────────────┐
  │ INTERFACE CHIP APPLIES THE DATA OF SOME OR ALL OF THE   │
  │ TESTS IN STEP 516 TO ALL DUTs                     618   │
  └────────────────────────────────────────────────────────┘
                   │
                   ▼
  ┌────────────────────────────────────────────────────────┐
  │ TESTER INITIATES READ CYCLES ON MULTIPLE TESTER         │
  │ CHANNELS, ACCORDING TO CONVENTIONAL TECHNIQUES    619   │
  └────────────────────────────────────────────────────────┘
                   │
                   ▼
  ┌────────────────────────────────────────────────────────┐
  │ INTERFACE CHIP READS DATA FROM DUTs AND PERFORMS        │
  │ CROSS-DUT AND/OR WITHIN-DUT COMPARISONS TO DETERMINE    │
  │ IF THERE ARE ANY ERRORS IN THE READ DATA AND OPTIONALLY │
  │ PERFORMS STATISTICS TO PREDICT ERRORS IN THE DUTs;      │
  │ APPROPRIATE ERROR STORAGE AND DATA COMPRESSION TAKES    │
  │ PLACE                                             620   │
  └────────────────────────────────────────────────────────┘
                   │
                   ▼
  ┌────────────────────────────────────────────────────────┐
  │ TESTER SENDS ADDRESSES ON MULTIPLE TESTER CHANNELS      │
  │ SIMULTANEOUSLY, REQUESTING TO READ THE ERROR DATA THAT  │
  │ WAS PRODUCED IN STEP 520                          624   │
  └────────────────────────────────────────────────────────┘
                   │
                   ▼
  ┌────────────────────────────────────────────────────────┐
  │ INTERFACE CHIP RESPONDS BY PROVIDING NEW ERROR          │
  │ INFORMATION CONCERNING EACH OF THE DUTs           628   │
  └────────────────────────────────────────────────────────┘
                   │
                   ▼
  ┌────────────────────────────────────────────────────────┐
  │ TESTER RECOGNIZES THE NEW ERROR INFORMATION, UPDATES    │
  │ THE STORED ERROR INFORMATION FOR EACH OF THE DUTs  632   │
  └────────────────────────────────────────────────────────┘
```

Fig. 6

Fig. 7
(Prior Art)

Fig. 8

(TO FIG. 9b)

**Fig. 9a**

Fig. 9b

Fig. 10

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DISTRIBUTED INTERFACE FOR PARALLEL TESTING OF MULTIPLE DEVICES USING A SINGLE TESTER CHANNEL

This is a Continuation application of Ser. No. 09/260,463, filed Mar. 1, 1999, U.S. Pat. No. 6,499,121.

The subject matter in this application is related to material in two other U.S. patent applications of Roy and Miller, entitled PARALLEL TESTING OF INTEGRATED CIRCUIT DEVICES USING CROSS-DUT AND WITHIN-DUT COMPARISONS, having Ser. No. 09/260,459 (P077), and EFFICIENT PARALLEL TESTING OF INTEGRATED CIRCUIT DEVICES USING A KNOWN GOOD DEVICE TO GENERATE EXPECTED RESPONSES, having Ser. No. 09/260,460 (P078), filed on the same date as this application and expressly incorporated herein by reference.

BACKGROUND INFORMATION

This invention is related to the testing of integrated circuit devices using a semiconductor tester, and more particularly to testing a number of devices in parallel using a single channel of the tester for greater efficiency and throughput.

Integrated circuit (IC) devices are an important part of almost every modern electronic or computer system. To reduce the manufacturing cost of such systems, the manufacturer expects each constituent IC device to be free of defects and to perform according to its specifications. Thus, it is not unusual to expect that every IC device is subjected to rigorous testing prior to being shipped to the system manufacturer.

It has been determined, however, that a significant portion of the total cost of producing an IC device can be attributed to its testing. That is because many modern IC devices perform complex functions, have a large number of inputs and outputs, and operate at high speeds. For instance, a 256 Mb memory device may have 16 data lines and 22 address lines. A simplistic approach to test such a device would be to write a known data value to each memory location, and then read from each location, and then compare the value read to the expected or written value to determine any errors. However, because of the large number of locations, each containing several bits, such a technique of testing each bit of each location is very time consuming. As a result, the field of test engineering has developed to create efficient techniques for detecting as many errors as possible while using the least number of test sequences.

A memory device may be tested using an automated semiconductor tester. FIG. 1 shows such a tester **108** having a number (N) of channels for parallel testing of a number of devices under test (DUTs) such as DUT **118**. The tester **108** normally executes a test program and in response generates data and addresses on each channel which define a complex test sequence **106** engineered for testing the particular DUTs. Each channel of the tester **108** feeds a respective DUT so that a number of DUTs, corresponding to the number of channels, are tested simultaneously. A probe card (not shown) receiving all N channels delivers address and write data of the test sequence **106** to locations in N different DUTs simultaneously, while the DUTs are still part of a semiconductor wafer **116**. The tester **108** then reads from those locations and performs a comparison with expected data it generates. The results of the comparison help determine whether a particular bit read from a location in a DUT is in error. The tester **108** performs the above read and write cycles many times with the same or different data patterns to verify as many locations of the DUTs as possible given time and budget constraints.

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To increase throughput in terms of the number of DUTs tested per unit time, a larger tester may be built having more channels. Such a solution, however, could be prohibitively expensive. The tester is a complex and high speed machine, requiring much time and expense to modify or improve. Moreover, a single channel of a modern tester may comprise between 50 to 100 signal wires, such that increasing the number of channels between the tester and the probe card will make it physically impractical to connect all of the signal wires to the probe card. Therefore, a more efficient solution for increasing the throughput of an IC test system is needed.

SUMMARY

Accordingly, an embodiment of the invention is directed to interface circuitry that essentially acts as a relay between the tester and a number of DUTs, where test vectors on each channel are fanned out to multiple DUTs. In general, the test vectors include stimuli, such as addresses, data values, and control signals, that are passed on to the DUTs while maintaining any timing constraints between the stimuli that were set up by the tester. The responses by the DUTs to these stimuli may then be collected by the interface circuitry and relayed back to the tester. If desired, the interface circuitry may be further enhanced with error detection capability based on the responses. For instance, the response from each DUT may be evaluated for internal consistency, by within-DUT and across-DUT comparisons, or it may be evaluated by comparison to expected responses received from the tester. The results of the comparison may then be provided back to the tester in summary or in detail form.

In a further embodiment, the interface circuitry features an input for receiving test data, expect data (test vectors), and control values from the tester. An output drives the test data into a number DUTs and then subsequently reads the data from the DUTs. Comparison circuitry provides error information in response to performing a comparison between data values read from each of the DUTs and expected data received from the tester. A storage area for the error information may be provided as part of the interface circuitry. The interface circuitry thus allows each channel of the conventional tester to be used to test not just a single DUT but a number of DUTs, preferably in parallel.

According to another embodiment of the invention, a system is disclosed for testing a number of DUTs, having a conventional tester with a number of sets of tester input/output (I/O) lines, the tester providing data values on each set of tester I/O lines for testing a single DUT, and a probe card having a number of probe elements for contacting a number of signal locations of two or more DUTs. The interface circuitry is aboard the probe card and has an input coupled to one of the sets of tester I/O lines and an output coupled to the probes. The interface circuitry transports data values from its input to its output, and performs a comparison using data values read from the DUTs to determine errors, if any, in the DUTs. Multiple DUTs may thus be tested by each channel of the tester, without disturbing the test sequence that was previously created to test a single DUT. The tester program inside the tester may be modified to read the error information through the same set of tester I/O lines after the test sequence has been completed.

In a particular embodiment, the results of the comparison (error information) are returned to the tester via the same channel in response to the tester requesting a read of previously written data. The tester program is modified to recognize that the error information received in response to its read request concerns a number of DUTs rather than just a single DUT.

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In a particular embodiment, the DUTs are memory devices and the error information represents a difference between a data value read from each of the memory devices and an expected data value received by the interface circuitry from the tester for a pre-defined address/location.

These as well as other features and advantages of various embodiments of the invention can be better appreciated by referring to the claims, written description, and drawings below.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a prior art system for testing IC devices, with one DUT per channel of the tester.

FIG. 2 shows a block diagram of a system for testing a number of DUTs by each channel of a conventional tester, according to an embodiment of the invention.

FIG. 3 illustrates a block diagram of an interface circuit according to an embodiment of the invention.

FIG. 4 shows a block diagram of tester-DUT interface circuitry for testing 16 DUTs simultaneously using a single channel of the tester, according to an embodiment of the invention.

FIG. 5 is a flow diagram of operations performed in a system for testing IC devices using expected data received form the tester, according to an embodiment of the invention.

FIG. 6 is a flow diagram for testing devices without receiving expected data from the tester.

FIG. 7 shows a conventional technique for testing a 16-bit word of a memory device.

FIG. 8 shows a technique for providing error values concerning four DUTs on a channel being 16-bits wide, using comparisons made across DUTs, according to another embodiment of the invention.

FIGS. 9a and 9b show a technique for testing four DUTs using a combination of within-word comparisons and across-DUT comparisons, according to another embodiment of the invention.

FIG. 10 illustrates a probe card according to another embodiment of the invention.

DETAILED DESCRIPTION

FIG. 2 illustrates an embodiment of the invention as a system for testing multiple DUTs using a single channel of a conventional semiconductor tester. The DUT may be an entire IC die, such as a memory chip, or it may, be an arbitrary semiconductor device having a memory portion. The DUTs are normally similar, and preferably identical, devices. The test system features an N channel tester 108 that operates according to a test program 206. The tester 108 may be part of an IC manufacturing and test line which features a system controller 104. The system controller 104 is responsible for orchestrating a process flow of manufacturing and test operations for the DUTs. While executing the test program 206, a test sequence 106 is followed and test vectors, including data values and associated addresses and perhaps other control signals, are provided on each channel according to conventional techniques. For instance, in the embodiment shown in FIG. 2, there are 22 address lines in address bus 244 and 16 data lines in data bus 240 (control signals not shown). Of course, one of ordinary skill in the art will recognize that other bus configurations and widths may alternatively, be used, depending on the overall performance desired and the particular type of DUT being tested. The data

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lines are used to transport the test sequence data to interface circuitry 226. In certain versions of the invention, the same data lines may be used to return error information back to the tester 108. This complies with the conventional bi-directional use of the data lines of a tester channel.

The interface circuitry 226 for each channel is divided into subcircuits 216a, 216b, . . . Each subcircuit 216 can drive a combination of inputs and monitor a combination of outputs of one or more DUTs. Each subcircuit 216, for this particular embodiment, is configured to communicate with four DUTs simultaneously. One of ordinary skill in the art will recognize that each subcircuit can be configured to interface with fewer than or greater than four DUTs. Each subcircuit 216 forwards a test vector received from the single channel to each of four DUTs. The data value and its associated address are applied to each of the DUTs, perhaps following an address mapping to corresponding addresses in each of the DUTs.

When the tester 108 enters a read cycle, the tester 108 provides expected data and associated addresses to each subcircuit 216. Each subcircuit 216 reads data from corresponding addresses in the DUTs. Comparisons are then performed by the subcircuit between the expected data and the read data to determine if the data read from the DUTs contains any errors. In certain cases, the subcircuit may be designed to provide the error information back to the tester 108 in real-time, such that the tester 108 can abort further testing. The tester may also collect the errors for subsequent analysis or for repair of a DUT, for example by selecting among redundant circuit elements in the DUT.

In a particular embodiment, the error information generated by the interface circuitry 226 is provided back to the tester 108 through the same channel that was used for receiving expected data. However, the added fan-out provided by the interface circuitry 226 restricts the number of bits that can be used to return error information simultaneously for all DUTs. For instance, when sixteen DUTs are being tested by a 16-bit (data bus) channel as shown in FIG. 1, only 1 bit of error information can be provided per DUT if each DUT is assigned a channel. The amount of error information that is necessary to return to the tester 108 may depend on the type of testing that the process flow requires. For instance, in final test, a simple "go-no go" bit per DUT may be adequate. When testing for redundant repair, the size and configuration of the repairable circuit elements influences the bandwidth of the error information that is required.

FIG. 3 shows a high level block diagram of the internal architecture of a tester-DUT interface subcircuit 216a. A channel address port 304 is provided to receive addresses from the address bus 244 and control signals from a control bus (not shown) of a single channel. A tester data I/O port 308 is provided to receive data values from the data bus 240 of the single channel. An expect data register 309 is clocked by a read control signal received from the channel's control bus (not shown) to latch the expected data. In this embodiment, four of the 16 lines of the data bus are used by the subcircuit 216a to return error information back to the tester 108 regarding four DUTs, 310a, 310b, 310c, and 310d. The remaining 12 lines will be used in a similar fashion by the other subcircuits 216b, 216c, and 216d.

On the DUT side, DUT I/O ports 314a, 314b, 314c, and 314d are provided as a data interface with their corresponding DUTs. Note that the 16 data bits received through the tester I/O port 308 are copied to all four DUT I/O ports which in turn forward the data to their respective DUTs. A number of DUT address ports 320a, 320b, 320c, and 320d

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are provided for delivering the received address or a mapped address to each respective DUT.

Comparison circuitry 330 receives read data from each respective DUT and performs a comparison to determine whether the read data exhibits any errors. In the embodiment of FIGS. 2–4, a 16:1 compression is performed by the comparison circuitry 330. This means that for every 16 bits of data at each location of a DUT, 1 error bit is generated by each subcircuit 216, such that for each address, 16 error bits in total are provided by the interface circuitry 226 on the data bus 240 of the tester channel. FIG. 4 shows a detail of four tester-DUT interface subcircuits 216a, 216b, 216c, and 216d and how they may be coupled to the address and data buses of a single tester channel. Each subcircuit 216 provides 4 bits of error information on the data bus, for a total of 16 bits corresponding to four sets of four DUTs each. Other ways of configuring the interface circuitry 226 for testing a greater number of DUTs simultaneously, using a single channel of the tester 108, may be devised by one of ordinary skill in the art. These configurations depend on the amount of error data required by the process flow. For instance, in a final test scenario, a single fail bit might be sufficient for each DUT. In other cases, a fail bit per address/location may be sufficient. Also, rather than using the parallel bus approach shown in FIG. 4, a serial link might alternatively be used to connect the interface circuitry 226 to the tester 108 or system controller 104.

Returning briefly to FIG. 2, the interface circuitry 226 may be part of a probe card 212 which is coupled to a separate channel of the tester 108. The probe card 212 shown in FIG. 2 provides a fan-out of M, so that its channel is coupled to M different DUTs simultaneously on a wafer 116. Therefore, a system using a conventional N-channel tester 108 normally capable of testing 16 DUTs, one DUT per channel, would be capable of testing M×N DUTs simultaneously if equipped with N probe cards.

FIG. 5 illustrates a flow diagram of the operations performed in a system for testing IC devices, according to an embodiment of the invention. Operation may begin with step 504 in which the tester 108 generates addresses and data for a test sequence to be applied as inputs to a single DUT. This may be done according to conventional test engineering techniques of generating a data value and an associated address on each channel of the tester 108. Operation proceeds in step 508 where the tester sends the data and associated address on multiple tester channels simultaneously, once again according to conventional techniques. Operation then proceeds with step 512 in which the interface circuitry 226 receives the data and addresses over a single channel, and in response applies the data to a number of DUTs simultaneously. The addresses presented to each of the DUTs may be the same as the addresses received from the tester. Alternatively, an address received from the tester 108 may be mapped to different, corresponding addresses/locations in the DUTs. This mapping allows the interface circuitry 226 to be configured for single DUT operation, where the tester 108, if so programmed, can access any location in any of the DUTs, preferably after the test sequence has been completed. The added latency due to the interface circuitry 226 when forwarding the data to the DUTs (which may not have been present when each channel was handling only a single DUT) may be easily handled by inserting a systematic delay between consecutive read or consecutive write commands in the test program or in the interface circuitry 226.

After the tester 108 has delivered the address and data over the channels, operation may proceed with step 516 in

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which the tester 108 may optionally run refresh cycles if the DUTs are memory devices, or arbitrary semiconductor devices including memory portions. In addition, long cycle tests and other test patterns which may be designed to stress the electrical parameters of the DUTs may be delivered to the interface circuitry 226, as in step 512. The interface circuitry 226 will normally be configured to mimic such sequences to all of the DUTs. Operation then proceeds with step 519 in which the tester sends an expected data value to the interface circuitry 226, while simultaneously initiating a read from each DUT. The expected data value and its associated address are normally the same as the data and address that were sent by the tester in step 508. Operation then proceeds with step 520 where the interface circuitry 226 latches the expected data from the channel, reads data from corresponding locations in the DUTs, and performs comparisons between the read data and the expected data to determine if there are any errors in the read data.

The results of such a comparison may then be compressed, sent back to the tester 108 or system controller 104, or stored in memory 399 (see FIG. 3). The error information may be returned to the tester either in real-time or as a post process, using the same channel over which the expected data arrived. The compression depends on the number of DUTs being tested by each channel and the width of the data bus in the channel. For instance, when sixteen DUTs are tested by each channel having a 16-bit data bus, a 16:1 compression may be performed so that 1 bit of error information is available per DUT. This, of course, means that if there is an error in 1 or more of the 16 bits at a given location read from a DUT, the exact bit location of the errors are not transmitted back to the tester in real time. If desired, the interface circuitry 226 may be configured with a bypass mode which allows the tester 108 to query any failed locations of any particular DUT to determine the exact bit locations of the error. This will typically be done following completion of the test sequence. Alternatively, the memory 399 may be used to collect the error data for post processing by the tester 108 or system controller 104.

FIG. 6 is a flow diagram of an alternative technique for determining error information using the interface circuitry 226, without delivering expected data over the tester channels. The interface circuitry may be configured to operate in this and, in general, in different modes in response to instructions received from the tester. See, for example, U.S. patent application of Ray and Miller entitled EFFICIENT PARALLEL TESTING OF INTEGRATED CIRCUIT DEVICES USING A KNOWN GOOD DEVICE TO GENERATE EXPECTED RESPONSES (P078). Operations 604–616 may be performed in the same manner as operations 504–516 in FIG. 5. Once the interface circuitry 226 has applied test data to its corresponding DUTs in step 618, operation continues with step 619 in which the tester 108 initiates a read cycle on each channel to read from the locations to which it previously wrote. The interface circuitry 226 responds in step 620 by reading from its corresponding DUTs, and performs comparisons of data values across DUTs and/or within DUTs to determine any errors in the DUTs. For instance, the interface circuitry 226 may be configured to perform comparisons of groups of bits read from locations within the same DUT, where each group had the same bit pattern written to them in step 618. Such a conventional technique is discussed below in connection with FIG. 7. In addition or instead of the conventional technique, the interface circuitry 226 can be further configured to perform comparisons of bits read from locations in different DUTs. This latter technique is described below in

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relation to FIG. 8. A combination of these two techniques of "within word" and "across DUT" comparisons is illustrated in FIGS. 9a and 9b. Thus, in contrast to the embodiment of FIG. 5, the tester 108 in FIG. 6 does not send expected data to the interface circuitry 226 during the test sequence. Rather, the interface circuitry 226 performs cross-DUT and within-DUT comparisons, such as in FIGS. 7–9 below, and optional statistics, to predict errors in the DUTs with relatively high confidence. Appropriate storage of the error data and compression also takes place. Eliminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology.

Regardless of which technique is used to generate the error information in step 520/620, operation continues in FIG. 5 with steps 524 and 528 (and corresponding steps 624 and 628 in FIG. 6) in which the interface circuitry 226 provides error information concerning each of the DUTs in response to a request from the tester 108 to read from particular addresses. Operation then continues with step 532/632 in which the tester 108, according to a modified test program, recognizes that the new error information relates to a number of DUTs rather than to a single DUT, and updates its stored error information for each of the DUTs accordingly. Steps 504–532 described above may be repeated many times as required by the test sequence 106 (see FIG. 1).

As mentioned above, step 520 in FIG. 5 involves performing a comparison by the comparison circuitry 330 (see FIG. 3) to determine if there are any errors in the read data obtained from the DUTs. Several techniques for performing the comparison are presented in this disclosure. One such technique that was introduced above configures the comparison circuit 330 to perform an exclusive OR (XOR) operation upon corresponding bits of an expected data value received from the tester 108 and of a read data value from a DUT.

In contrast, FIG. 7 shows a conventional technique for performing a comparison within a location or data word of a DUT. The objective here is to obtain a 4-bit compressed error value that represents errors, if any, in a 16-bit word of a single DUT. Using this technique, 4 DUTs may be tested in parallel so that 16 bits of error data can be returned to the tester 108 through a 16-bit data bus of the channel. In FIG. 7, a 16-bit data word to be compared is divided into four groups of 4 bits referenced W, X, Y, and Z. In this case, it is assumed that the pattern of data that was written to this data word repeats every 4 bits such that each group should have the identical bit pattern. In the particular example of FIG. 7, CIOW, CIOX, CIOZ all indicate a positive result. This means that all of the W, X, and Z bits in the data word are correct. In contrast, CIOY indicates a negative result for bit location Y, without specifying which group contains the error in bit Y. Although this type of compressed error information provides an incomplete picture of the errors encountered in a data word, it may nonetheless be useful in certain situations where, for instance, the DUT contains redundant circuitry that can replace the circuitry which provided the failing Y bits.

One drawback of the conventional approach in FIG. 7 is that a false positive result of a comparison CIO could be generated when all corresponding bits of a given location are in error. For instance, With CIOY indicating a negative result, at most 1, 2, or 3 of the four corresponding Y bits can be in error. If all four of the Y bits were in error, however, then CIOY would indicate a positive result, because all four inputs to its XOR gate would have the same value. Although it is a rare case Where all four corresponding bits are in error,

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it is desirable to eliminate or at least reduce the occurrence of such a false positive result. This could be accomplished by configuring the interface circuitry 226 into a bypass mode and running a conventional test using tester 108 to test a single device of the multiple devices for absolute accuracy.

FIG. 8 illustrates another technique of performing a comparison. Such a technique involves comparing bits from different DUTs. Although FIG. 8 shows comparing across 4 DUTs, the concept may be implemented with any number of DUTs, within practical limitations, of course. Once again, this scheme assumes that the comparisons made by each XOR gate are of bit values that should be the same, such that a positive result is generated only if all bits have the same 0 or 1 value. For this example, each data word comprises 16 bits. The first XOR gate 880 provides a Compare Across DUTs of bit 0 in each of the DUTs (CAD0). Similarly, CAD1 from XOR gate 881 gives the result of comparing bit 1 in each of the DUTs and so on until CAD15 provided by XOR gate 895. In contrast to the repetitive pattern required for the conventional technique in FIG. 7, this approach allows an arbitrary pattern of data to be written in each word. However, the CAD result does not indicate which DUT contains the error, but only that one or more bits are in error. The CAD result will give a false positive result if 4 corresponding bits in 4 different DUTs are all in error. As mentioned previously, this situation can be avoided by testing at least one of the DUTs for absolute accuracy using the bypass mode.

FIGS. 9a and 9b illustrate a combination of within word and across DUT comparisons which increases the confidence in a positive result by several orders of magnitude over either the conventional technique of FIG. 7 or the across DUT comparison in FIG. 8. The schematic in FIGS. 9a and 9b shows the comparison circuitry for bit W which is the first of 4 bits in a group, where each data word comprises 4 such groups. Thus, the circuitry shown in FIGS. 9a and 9b will be repeated 3 times to provide the results of comparisons for bits X, Y, and Z.

The first series of XOR gates 910, 912, 914, and 916 provide the results CIOW0, CIOW1, CIOW2, and CIOW3, respectively. CIOW0 is the result of a within word comparison of bits W in a single word of DUT0. Similarly, CIOW1 is the result of a comparison of bit W in a single word of DUT1, and so on.

The second series of exclusive OR gates in FIGS. 9a and 9b are 920, 922, 924, and 926 providing CADW0, CADW1, CADW2, and CADW3, respectively. CADW0 is a comparison of bits W in set 0 of each DUT, CADW1 compares bits W in set 1 of each DUT, and so on. Thus, the CADW result is similar to the CAD result of FIG. 8 except that only 4 bits (the W bits) are compared.

Finally, the third series of gates in FIGS. 9a and 9b are 930–945, a total of 16 NOR gates each providing an OKW_result. The first 4 results OKW00_ to OKW03_ indicate errors, if any, in bits 1 of one or more of the 4 sets that define a word in DUT0. Similarly, OKW10_ to OKW13_ indicate errors in bits W of the 4 sets that define a corresponding word of DUT1, and so on. Note that the exact location of the error is given, i.e., no compression is performed, because one bit is used to indicate an error in bit W of a particular set in a data word in a given DUT. When the circuitry of FIGS. 9a and 9b is repeated for bits X, Y, and Z, a total of 16×4=64 error bits are available to exactly indicate errors in any bit of a data word, in any given DUT.

If desired to return error information concerning two or more DUTs back to the tester 108 over a single channel,

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compression may be performed to reduce the 16 bits of error information into 4 bits in order to efficiently use a 16-bit address bus of the channel. For instance, with only 4 bits of compressed error data for each DUT, each bit indicates an error, if any, in a corresponding 4-bit set of a 16-bit data word. As mentioned before, the tester **108** may nonetheless make valuable use of such information, for example by repairing the DUT if redundant circuitry is available in the DUT to replace a failed circuit.

FIG. 10 illustrates a probe card **1000** comprising subcircuits **216a** and **216b** of the interface circuitry **226**, according to another embodiment of the invention. The probe card **1000** features a number of probe elements **1004** for electrically connecting signal points of a DUT to its respective subcircuit. The probe elements **1004** are attached to a space transformer **1008** on the opposite side of which the IC die of the subcircuits are attached. Signals are transported to and from a controlled impedance tester interface board **1012** using a resilient interposer **1016**. The tester channel appears as traces in the interface board **1012**. The space transformer **1008** and the interface board **1012** are normally kept at a fixed relationship with each other, such as by using fasteners **1024**. A planarizer **1020** may be provided to place all of the probe elements into planar alignment with the wafer **116** under test. In operation, the probe card is lowered on to the surface of the wafer **116** for the probe elements to contact the signal points of the DUTs that form the wafer. Further details concerning this embodiment may be found in U.S. patent application Ser. No. 08/554,902, filed Nov. 19, 1995, entitled, *Probe Card Assembly With Space Transformer and Interposer*, or in the corresponding PCT application published May 23, 1996 as WO96/15458(P006).

To summarize, various embodiments of the invention for testing a number of DUTs in parallel using a single channel of a conventional tester have been disclosed. One of ordinary skill in the art will recognize that the invention is capable of use in various other combinations and environments and is capable of changes and modifications within the scope of the inventive concept expressed here. For instance, the interface circuitry described in different embodiments above would normally be implemented as one or more integrated circuit chips, each corresponding to a subcircuit, that reside on a probe card. In this way, the drive and sense electronics in the DUT ports are physically closer to the actual DUTs, thereby providing a less problematic and more cost effective electrical connection between the DUTs and the comparison circuitry. An alternative to the wafer probe card embodiment would be to place the interface circuitry upon a test fixture between the tester channel and a tray of packaged IC devices, where each DUT is part of a packaged device rather than a portion of a wafer. Accordingly, it is intended that all such modifications and/or changes be within the scope of the claims.

What is claimed is:

1. A probe card assembly comprising:

a plurality of electrical contacts configured to make electrical connections with a semiconductor tester;

a plurality of probes disposed to contact a plurality of semiconductor devices to be tested; and

interface circuitry comprising:

receiving circuitry configured to receive from said semiconductor tester through ones of said electrical contacts test data, a location in one of said semiconductor devices, and expected response data;

writing circuitry configured to write through ones of said probes copies of said test data to said location in at least two of said plurality of semiconductor devices; and

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reading circuitry configured to read through ones of said probes actual response data generated by each of said at least two of said semiconductor devices in response to said test data.

2. The probe card assembly of claim 1, wherein said interface circuitry further comprises comparing circuitry configured to compare said expected response data received from said tester with said actual response data read from each of said at least two semiconductor devices.

3. The probe card assembly of claim 2, wherein said interface circuitry further comprises transmitting circuitry configured to transmit through ones of said tester electrical contacts a result of said comparison of said expected response data received from said tester with said actual response data read from each of said at least two of said semiconductor devices.

4. The probe card assembly of claim 2, wherein said interface circuitry further comprises an electronic memory configured to store a result of said comparison of said expected response data with said actual response data read from each of said at least two of said semiconductor devices.

5. The probe card assembly of claim 1 further comprising:

an interface board on which said electrical contacts are disposed; and

a space transformer on which said probes are disposed.

6. The probe card assembly of claim 5, wherein at least one of said receiving circuitry, said writing circuitry, and said reading circuitry is disposed on said space transformer.

7. The probe card assembly of claim 5, wherein said receiving circuitry, said writing circuitry, and said reading circuitry compose one or more integrated circuit chips.

8. The probe card assembly of claim 7, wherein each of said one or more integrated circuit chips is disposed on said space transformer.

9. The probe card assembly of claim 8, wherein said plurality of probes is disposed on a first surface of said space transformer, and each of said one or more integrated circuit chips is disposed on a second surface of said space transformer.

10. The probe card assembly of claim 9, wherein said first surface of said space transformer is opposite said second surface of said space transformer.

11. The probe card assembly of claim 1, wherein said plurality of probes is configured to contact said plurality of semiconductor devices while said semiconductor devices are in unsingulated wafer form.

12. A probe card assembly comprising:

tester interface means for making electrical connections with a semiconductor tester;

probe means for contacting a plurality of semiconductor devices to be tested;

receiving means for receiving through said tester interface means test data, a location in one of said semiconductor devices, and expected response data;

writing means for writing through said probe means copies of said test data to said location in at least two of said plurality of semiconductor devices; and

reading means for reading through said probe means actual response data generated by each of said at least two of said semiconductor devices in response to said test data.

13. The probe card assembly of claim 12 further comprising comparing means for comparing said expected response data received from said tester with said actual response data read from each of said at least two semiconductor devices.

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14. The probe card assembly of claim 13 further comprising transmitting means for transmitting through said tester interface means a result of said comparison of said expected response data received from said tester with said actual response data read from each of said at least two of said semiconductor devices.

15. The probe card assembly of claim 13 further comprising memory means for storing a result of said comparison of said expected response data received from said tester with said actual response data read from each of said at least two of said semiconductor devices.

16. A method of testing a plurality of semiconductor devices comprising:

  generating at a semiconductor tester test data and location data identifying a location on one of said semiconductor devices;

  transmitting said test data and said location data to a probe card assembly;

  writing said test data from said probe card assembly to said location on at least two of said semiconductor devices;

  generating at said semiconductor tester expected response data;

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transmitting said expected response data to said probe card assembly; and

reading at said probe card assembly actual response data from each of said at least two of said semiconductor devices.

17. The method of claim 16 further comprising comparing at said probe card assembly said expected response data received with said actual response data read from each of said at least two semiconductor devices.

18. The method of claim 17 further comprising transmitting from said probe card assembly to said semiconductor tester a result of said comparison of said expected response data with said actual response data read from each of said at least two of said semiconductor devices.

19. The method of claim 17 further comprising storing at said probe card assembly a result of said comparison of said expected result data with said actual result data read from each of said at least two of said semiconductor devices.

20. The method of claim 16, wherein said plurality of semiconductor devices are in unsingulated wafer form.

*   *   *   *   *

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(12) **United States Patent**
Miller

(10) Patent No.:   **US 6,784,674 B2**
(45) **Date of Patent:**   **Aug. 31, 2004**

(54) **TEST SIGNAL DISTRIBUTION SYSTEM FOR IC TESTER**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(52) **U.S. Cl.** **324/754**; 324/760
(58) **Field of Search** 324/754, 757–758, 324/760, 762, 765; 714/724, 734, 738, 742; 333/33, 246–247

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(57)   **ABSTRACT**

A probe board provides signal paths between an integrated circuit (IC) tester and probes accessing terminals on the surfaces of ICs formed on a semiconductor wafer for receiving test signals form the IC tester. A branching signal path within the probe board distributes a test signal produced by one channel of the IC tester to several probes. Resistors within the branching signal path resistively isolate the probes from one another so that a fault occurring at any one IC terminal will not affect the logic state of the test signal arriving at any other IC terminal. The isolation resistors are sized relative to signal path characteristic impedances so as to substantially minimize test signal reflections at the branch points.

32 Claims, 6 Drawing Sheets
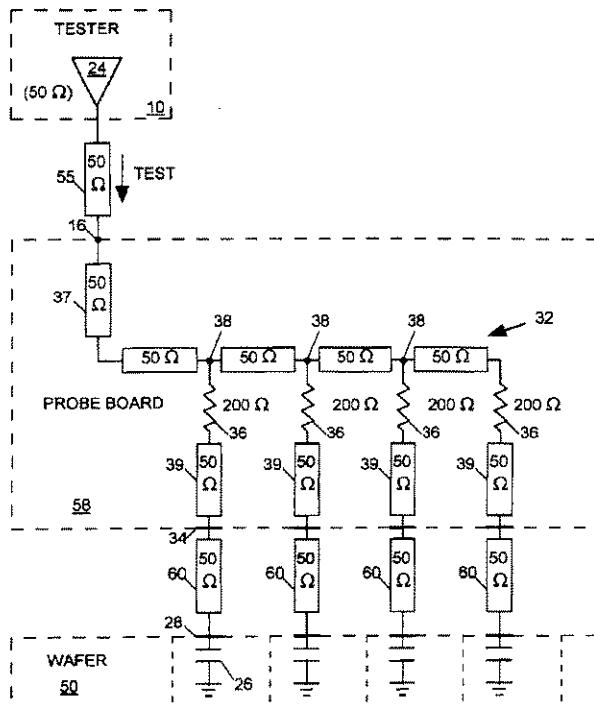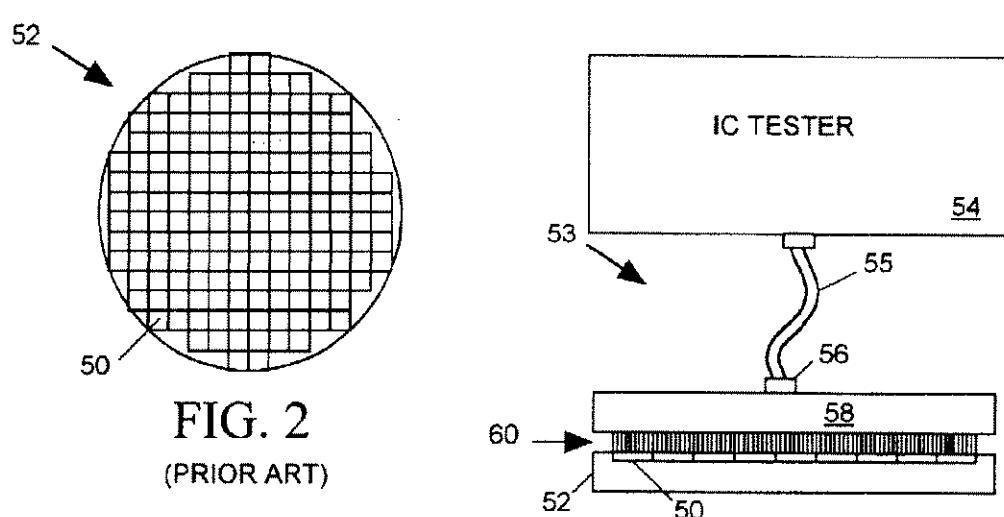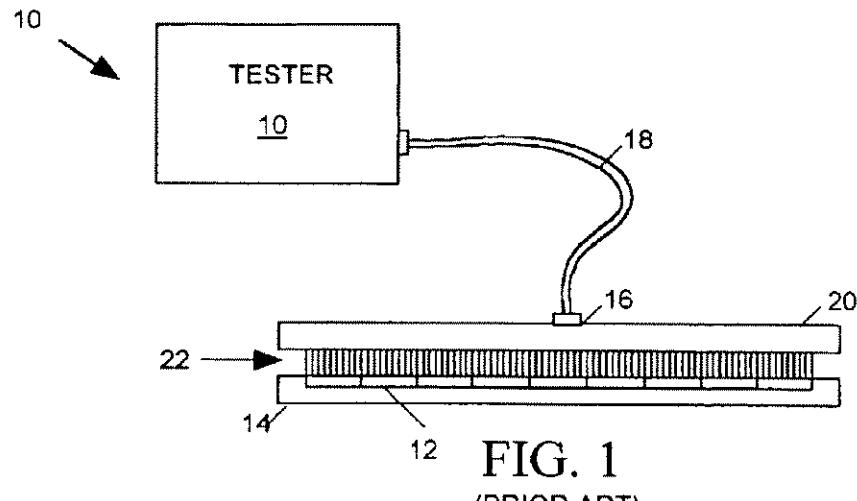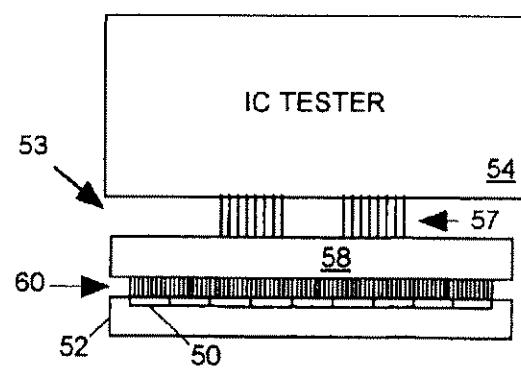
FIG. 1
(PRIOR ART)

FIG. 2
(PRIOR ART)

FIG. 3A

FIG. 3B

FIG. 4

FIG. 5

FIG. 6

TEST

50
Ω

FIG. 7

100 Ω   100 Ω

82

50   50
Ω   Ω

100 Ω   100 Ω   100 Ω   100 Ω

84   86

50   50   50   50
Ω   Ω   Ω   Ω

PROBES
TO IC PADS

TEST

50
Ω   FIG. 8

88

100   100
Ω   Ω

200 Ω   200 Ω   200 Ω   200 Ω

90   92
50   50   50   50
Ω   Ω   Ω   Ω

PROBES
TO IC PADS

FIG. 9

FIG. 10   FIG. 11   FIG. 12

FIG. 13
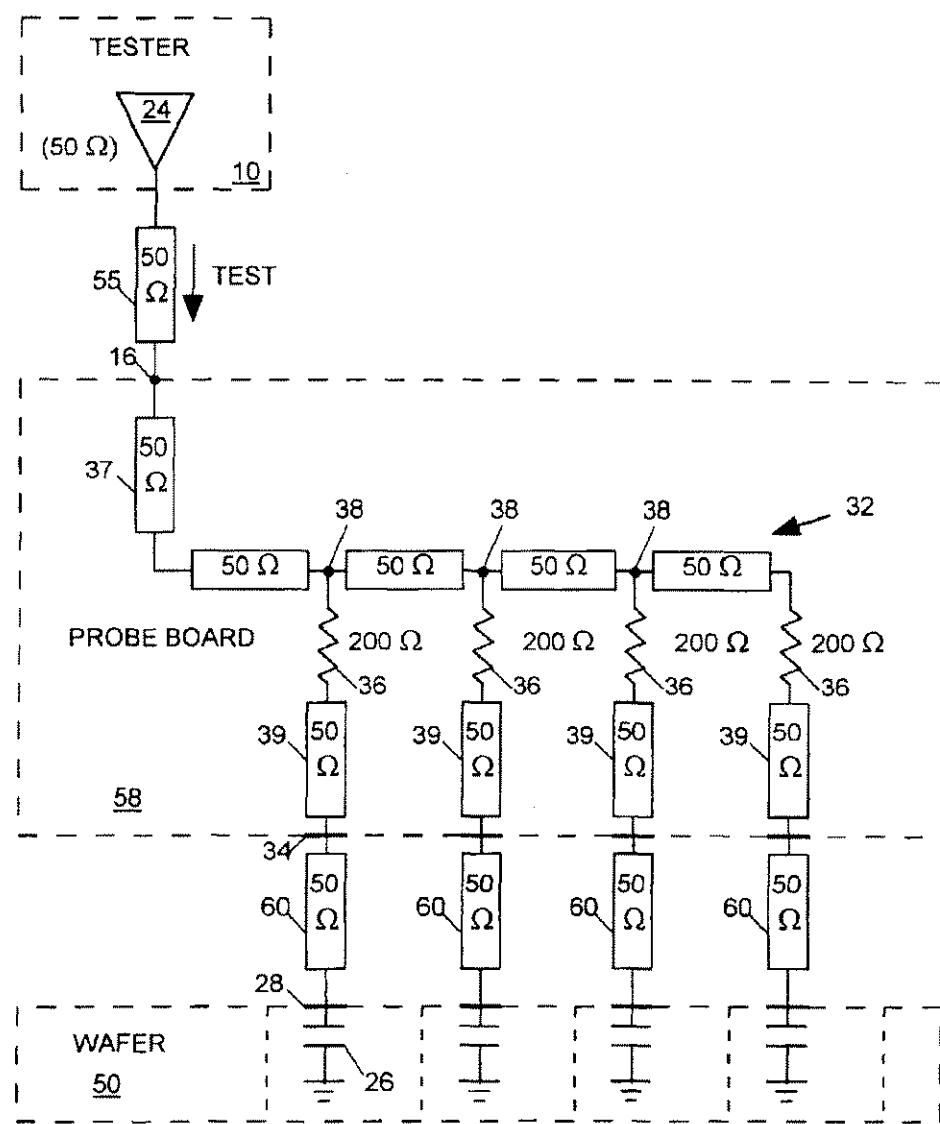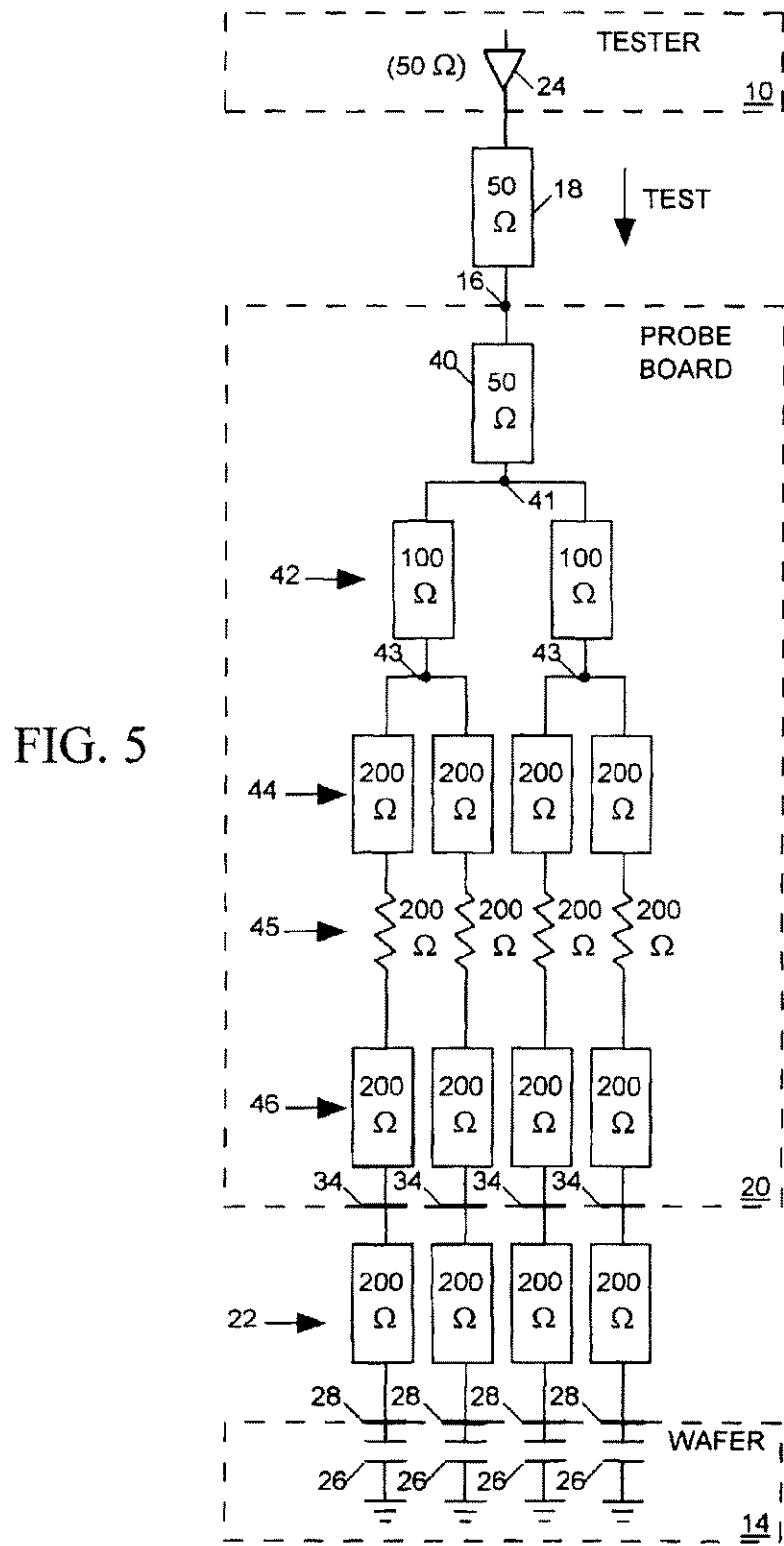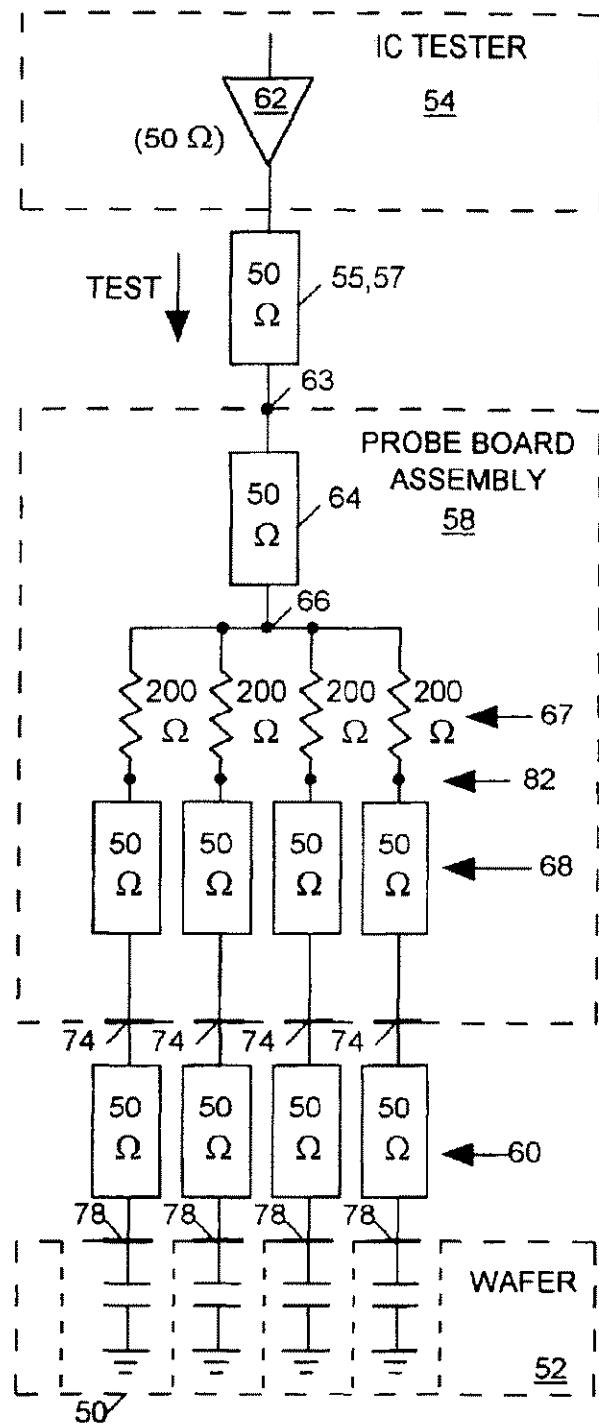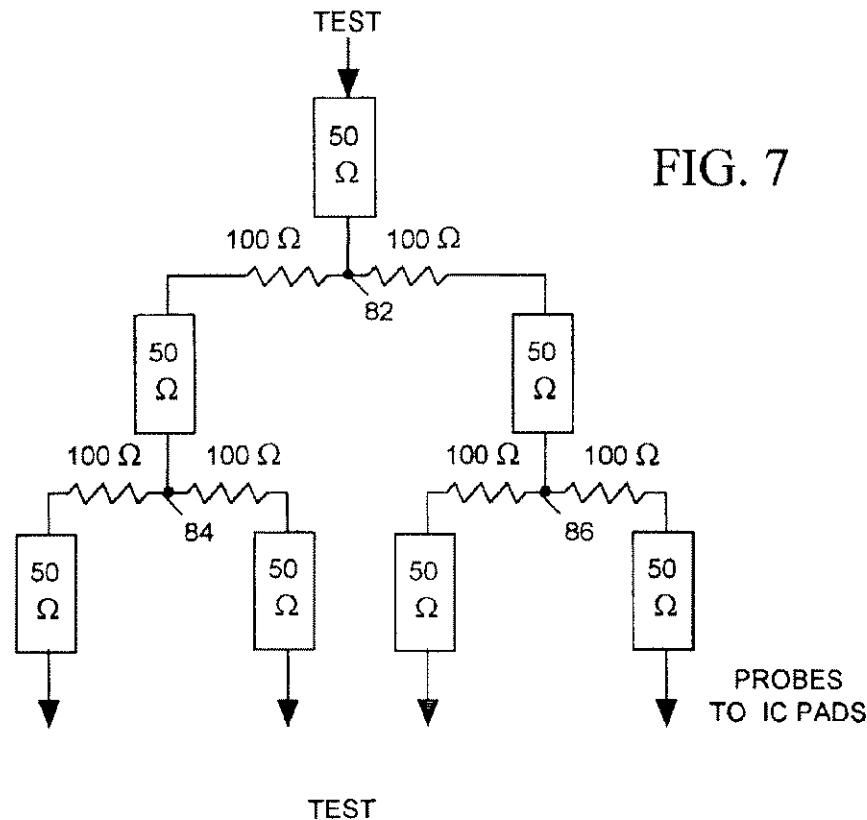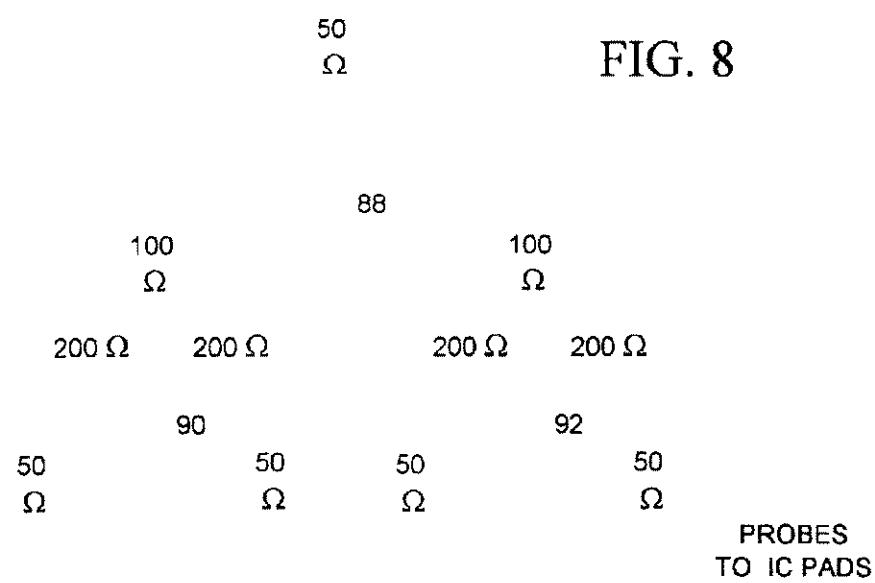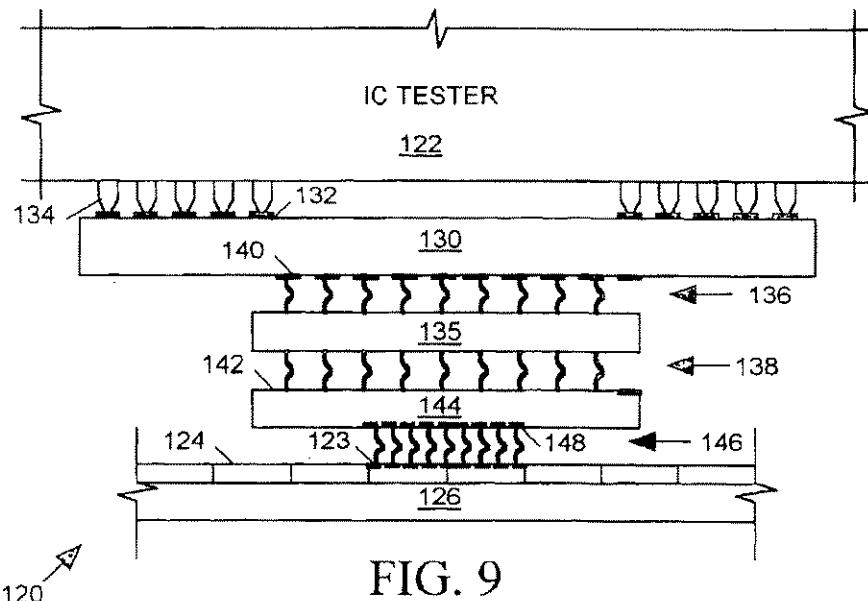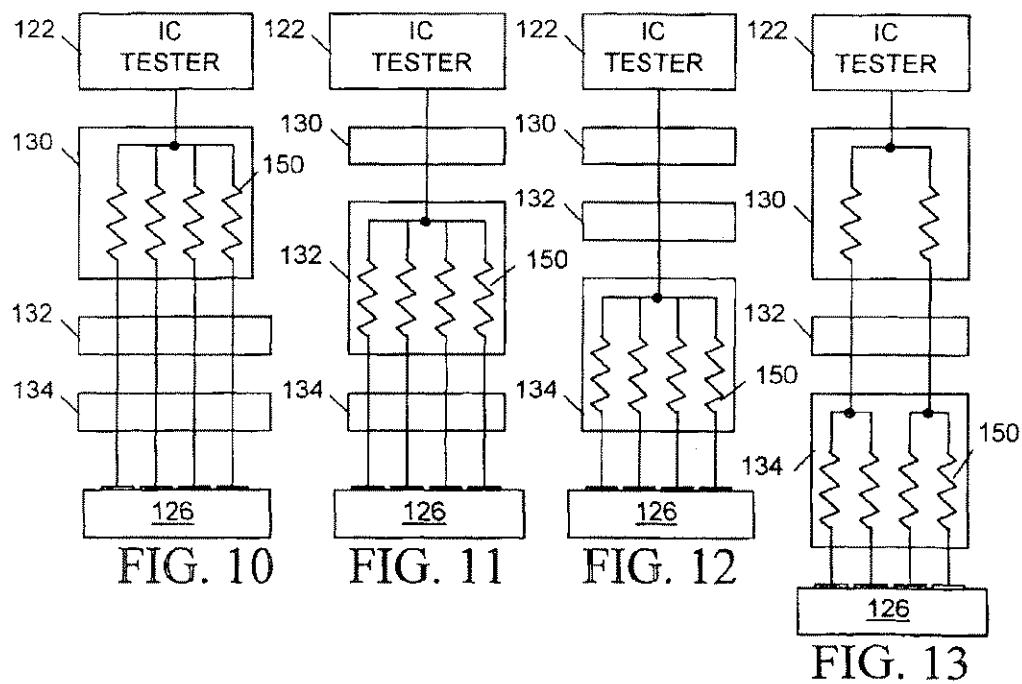
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TEST SIGNAL DISTRIBUTION SYSTEM FOR IC TESTER

FIELD OF THE INVENTION

The invention relates in general to interconnect systems for providing signal paths between an integrated circuit (IC) tester and pads on the surfaces of ICs, and in particular to a system for distributing a single test signal output of an IC tester to multiple pads on one or more ICs.

DESCRIPTION OF RELATED ART

An integrated circuit (IC) manufacturer fabricates an array of similar integrated circuits on a semiconductor wafer and then cuts the wafer to separate the ICs from one another. The ICs include pads on their upper surfaces providing points of contact for signal paths conveying IC output signals to other circuits or for receiving IC input signals from other circuits. The manufacturer may mount an IC in a package using bond wires to link the pads on the surface of the IC to package pins providing signal paths to external circuits. An IC can also be mounted directly on a printed circuit board (PCB) either by soldering pads on its surface to correspondingly arranged contact pads on the surfaces of the PCB or by providing spring contacts between pads on the surface of the ICs and the PCB's contact pads. The spring contacts may be attached to the IC's input/output (I/O) pads on the IC with their tips contacting the PCB's pads, may be attached to the PCB's pads with their tips contacting the IC's I/O pads, or may be attached to both the IC and PCB pads.

ICs are often tested at the wafer level before they are separated from one another. For example, as illustrated in FIG. 1, an IC tester 10 for testing ICs 12 residing on a wafer 14 includes a set of tester channels, each of which may either transmit a test signal to an IC I/O pad or monitor an IC output signal appearing at an IC I/O pad to determine whether the IC responds correctly to its input signals. A bundle of coaxial cables 18 provides separate signal paths between the input/output terminal of each tester channel and a cable connector 16 on a probe board assembly 20. A set of probes 22 connects pads on the lower surface of probe board assembly 20 to the pads on the upper surfaces of ICs 12. While coaxial or other kinds of cables 18 have been used to link a tester 10 to a probe board assembly 20 as illustrated in FIG. 1, pogo pin connectors have also often been used to provide signals paths between an IC tester and a probe board assembly.

Various types of structures can be used to implement probes 22 including, for example, wire bond and lithographic spring contacts, needle probes, and cobra probes. When spring contacts are employed to implement probes 22, they can be formed on the I/O pads of ICs 12 when probe board assembly 20 includes pads on its lower surface arranged to contact the tips of the spring contacts. U.S. Pat. No. 6,064,213, issued May 16, 2000 to Khandros et al (incorporated herein by reference), exemplifies such a probe board assembly.

When spring contacts are not formed on the I/O pads of ICs 12, they can be formed on the lower surface of probe board assembly 20 and arranged so that their tips contact the I/O pads of ICs 12. U.S. Pat. No. 5,974,662 issued Nov. 2, 1999 to Eldridge et al (incorporated herein by reference) describes an example of a probe board assembly employing spring contact probes. The following documents (also incorporated herein by reference) disclose various exemplary methods for manufacturing spring contacts: U.S. Pat. No.

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6,336,269 issued Jan. 8, 2002, to Eldridge et al., U.S. Pat. No. 6,255,126 issued Jul. 31, 2001 to Mathieu et al., U.S. patent application Ser. No. 09/710,539 filed Nov. 9, 2000, and U.S. patent application Ser. No. 09/746,716 filed Dec. 22, 2000.

Probe board assembly 20 provides signal paths between cable connectors 16 and the pads on the lower surface of probe board assembly 20 that probes 22 contact. Some probe board assemblies 20 are formed by multiple-layer printed circuit board having traces formed on the various layers for conveying signals horizontally and vias for conveying signals vertically though the layers. Other probe board assemblies include several separate substrate layers interconnected through spring contacts. See for example, U.S. Pat. No. 5,974,662 issued Nov. 2, 1992 to Eldridge, et al, incorporated herein by reference.

To test all ICs 12 on wafer 14, the channels within tester 10 must be able to access all I/O pads of all ICs. For example, ICs 12 might be random access memories (RAMs), with each RAM having eight I/O pads acting as an 8-bit address input, another eight I/O pads acting as an 8-bit data input/output, and one or more additional I/O pads for receiving input control signals. To test such a RAM IC, tester 10 writes data to each of its addresses, reads the data back out of each address and determines whether the data read out of the RAM matches the data written into it.

Thus tester 10 might include seventeen or more channels for each RAM IC to be tested, including eight channels for supplying signals conveying the 8-bit address, eight bi-directional channels for transmitting and receiving the 8-bit data, and one or more additional channels for providing the RAM's control signal inputs. However since a wafer 14 typically includes a large number of ICs 12, tester 10 would require a very large number of channels to concurrently test all of the ICs. Thus wafer-level IC testers typically test only a portion of the ICs of a wafer at a time, with the wafer being repositioned under the probes after each group of ICs is tested so that a next group of ICs can be tested.

What is needed is an inexpensive interconnect system that can distribute a test signal from an IC tester to pads of several ICs at the same time without causing substantial distortion due to signal reflection, and without requiring transmission lines having more than one characteristic impedance.

BRIEF SUMMARY OF THE INVENTION

The invention relates to an interconnect system for providing signal paths between an integrated circuit (IC) tester and input/output (I/O) pads of ICs formed on a semiconductor wafer so that the IC tester can test the ICs. The interconnect system includes a set of probes for accessing the I/O pads and a probe board assembly providing signal paths for conducting signals between the IC tester and the probes.

In accordance with an embodiment of the invention, a branching signal path within the probe board distributes a test signal produced by one channel of the IC tester to several probes. Isolation resistors within the branching signal path resistively isolate the probes from one another with sufficient resistance that a fault at any IC terminal connecting that IC terminal to a potential source through a low impedance path will not affect the logic state of the test signal arriving at any other IC terminal.

The isolation resistors are also sized relative to characteristic impedances of signal paths in which they reside so as to substantially minimize test signal reflections at the branch

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points. For example a set of four 200 Ohm isolation resistors are provided at a branch node between a 50 Ohm incoming transmission line and a set of four outgoing transmission lines since the parallel combination of four 200 Ohm resistors provides an equivalent 50 Ohm impedance matching the impedance of the incoming transmission line.

An impedance mismatch can occur between each isolation resistor and the outgoing signal path to which it is linked, as for example when each 200 Ohm isolation resistor is connected to a 50 Ohm outgoing transmission line. Such an impedance mismatch causes the junction between each isolation resistor and an outgoing transmission line to reflect a portion of the test signal as it travels toward a probe. However the isolation resistors are sufficiently large to attenuate such reflections so that they do not substantially distort the test signal upstream of the isolation resistors. Thus a reflection of a test signal in any one branch of the path adds little distortion to the test signal passing into any other branch of that path.

The claims appended to this specification particularly point out and distinctly claim the subject matter of the invention. However those skilled in the art will best understand both the organization and method of operation of what the applicant(s) consider to be the best mode(s) of practicing the invention, together with further advantages and objects of the invention, by reading the remaining portions of the specification in view of the accompanying drawing(s) wherein like reference characters refer to like elements.

BRIEF DESCRIPTION OF THE DRAWING(S)

FIG. 1 is a simplified side elevation view of a prior art probe board assembly providing an integrated circuit (IC) tester with access to input/output pads of a set of ICs formed on a semiconductor wafer;

FIG. 2 is a simplified plan view of a prior art semiconductor wafer containing an array of ICs;

FIGS. 3A and 3B are a simplified side elevation views of a probe board assembly in accordance alternative embodiments of the invention for providing an integrated circuit (IC) tester with access to input/output pads of a set of ICs formed on a semiconductor wafer;

FIGS. 4–8 are schematic diagrams alternative embodiments of a signal path in accordance with the invention between a channel of the tester of FIG. 3A or 3B and pads on the wafer of FIG. 3A or 3B;

FIG. 9 is a simplified side elevation view of a probe board assembly in accordance and alternative embodiment of the invention for providing an integrated circuit (IC) tester with access to input/output pads of a set of ICs formed on a semiconductor wafer; and

FIGS. 10–13 are schematic diagrams alternative embodiments of a signal path in accordance with the invention between a channel of the tester of FIG. 3A or 3B and pads on the wafer of FIG. 9.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS OF THE INVENTION

The present invention relates to an interconnect system for routing a test signal from a driver in one channel of an integrated circuit (IC) tester to more than one IC input/output (I/O) pad. The specification below describes one or more exemplary embodiments and/or applications of the invention considered by the applicant(s) to be the best modes of practicing the invention.

As illustrated in FIG. 2, an integrated circuit (IC) manufacturer initially forms an array of ICs 50 on a semiconduc-

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tor wafer 52. The wafer is thereafter cut to separate the ICs so that they can be separately packaged or mounted on printed circuit boards. However it is advantageous to test the ICs before they are separated from one another.

FIGS. 3A and 3B are simplified side elevation views of alternative embodiments of an interconnect system 53 in accordance with the invention for providing signal paths between an integrated circuit tester 54 and the I/O pads of a set of ICs 50 formed on semiconductor wafer 52 of FIG. 2. A set of tester channels within tester 54 transmit test signals through interconnect system 53 to I/O pads of ICs 50. Interconnect system 53 also returns output signals ICs 50 produce at their I/O pads in response to the test signals to tester 10 and tester 10 monitors those output signals to determine whether the ICs are behaving as expected.

Interconnect system 53 includes a probe board assembly 58 providing a large number of signal paths between its upper and lower surfaces. A variety of structures may be used to provide signal paths between tester 54 and the upper surface of the probe board assembly 58. For example, as illustrated in FIG. 3A, interconnect system 53 includes a set of coaxial cables 55 providing signal paths between tester 54 and a connector 56 on the upper surface of probe board assembly 58. Alternatively, as illustrated in FIG. 3B, interconnect system 53 may employ a set of pogo pins 57 to provide signal paths between tester 54 and pads on the upper surface of probe board assembly 58. The coaxial cables 55 and pogo pins 57 are exemplary; those of skill in the art will appreciate that other types of conductors can be used to provide signal paths between tester 54 and probe board assembly 58.

A set of probes 60 link pads on the lower surface of probe board assembly 58 to the I/O pads on the surfaces of ICs 50. Various kinds of probes known to those of skill in the art may implement probes 60 including, but not limited to, wire bond and lithographic spring contacts, needle probes, and cobra probes. When spring contacts are employed to implement probes 60, they can be formed on the I/O pads of ICs 50 when probe board assembly 58 includes pads on its lower surface arranged to contact the tips of the spring contacts. U.S. Pat. No. 5,974,662 issued May 16, 2000 to Khandros et al (incorporated herein by reference) exemplifies such a probe board assembly.) When spring contacts are not formed on the I/O pads of ICs 50, they can be formed on the lower surface of probe board assembly 58 and arranged so that their tips contact the I/O pads of ICs 50.

U.S. Pat. No. 5,974,662 issued Nov. 2, 1999 to Eldridge et al. (incorporated herein by reference) describes an example of a probe board assembly employing spring contact probes. U.S. patent application Ser. No. 09/810,871 filed Mar. 16, 2001 (incorporated herein by reference) also describes an example of a probe board assembly employing spring contact probes. The following documents (incorporated herein by reference) disclose various exemplary methods for manufacturing spring contacts: U.S. Pat. No. 6,336,269 issued Jan. 8, 2002 to Eldridge et al., U.S. Pat. No. 6,255,126 issued Jul. 31, 2001 to Mathieu et al., U.S. patent application Ser. No. 09/710,539 filed Nov. 9, 2000, and U.S. patent application Ser. No. 09/746,716 filed Dec. 22, 2000.

Probe board assembly 58 may, for example, be implemented by a single substrate having one or more layers with microstrip or stripline traces formed on or between the layers acting as transmission lines for conveying signals horizontally and vias for conveying the signal vertically through the layers. Alternatively substrate layers of the

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probe board assembly **58** may be vertically spaced from one another with spring contacts or other interconnect structures providing signal paths between the separate layers boards as illustrated, for example, in U.S. Pat. No. 5,974,662 issued to Eldridge, et al. Nov. 2, 1999 (incorporated herein by reference).

When one of the ICs **50** under test produces an output signal at one of the I/O pads on its upper surface, the output signal passes through one of probes **60** to a pad on the lower surface of probe board assembly **58** and then passes through a path provided by the probe board assembly and through cables **55** or pogo pins **57** to a receiver within a channel of tester **54**. Conversely when a driver within tester **54** sends a test signal outward via one of cables **55** or pogo points **57** to probe board assembly **58**, the test signal travels through a path provided by the probe board assembly **58** to one (or more) of probes **60**. The probe or probe(s) **60** then conveys the test signal to one or more I/O pads on the surface of one or more of ICs **50**.

To fully test every IC **50** on wafer **52**, tester **54** must be able to access every I/O pad of every IC. Since wafer **52** may include a large number of ICs **50**, and since each IC **50** may have a large number of I/O pads, tester **54** requires a large number of channels in order to concurrently test all ICs **50** on wafer **52**. To reduce the number of channels needed to test ICs **50**, a probe board assembly **58** distributes the test signal output of any one tester channel to corresponding I/O pads of more than one IC **50**, to multiple I/O pads on a single IC, or to a combination of the foregoing. The invention relates in particular to the nature of the signal path probe board assembly **58** provides for distributing a single test signal to several probes **60**.

In accordance with the invention, the number of tester channels needed is reduced by employing one channel of tester **54** to drive corresponding inputs of several ICs. For example, when the ICs to be tested are RAMs, each having an 8-bit input address, a set of eight tester channels supplies the same 8-bit input address concurrently to several RAM ICs. Similarly a control signal generated by a single tester channel can be distributed to control inputs of several RAM ICs.

FIG. **4** is a schematic representation of a network implemented within probe board assembly **58** of FIG. **3A** or **3B**, for distributing a test signal generated by a driver **24** of a single tester channel within tester **54** to corresponding I/O pads **28** of four separate ICs **50**. Since the input impedance of each I/O pad **28** is primarily capacitive (typically about 2 picofarads), the input impedance of each pad **28** is modeled in FIG. **4** by a 2 picofarad capacitor **26**. One of the coaxial cables **55** of FIG. **3A** (or pogo pins **57** of FIG. **3B**) linking driver **24** to a connector (or pad) **16**, represented in FIG. **4** as a circuit node. Since the output impedance of a tester driver is typically 50 Ohms, a coaxial cable **55** (or pogo pin **57**) having a matching 50 Ohm characteristic impedance is used. FIG. **4** depicts cable **55** as a transmission line having a 50 Ohm characteristic impedance. Probe board assembly **58** provides signal paths linking node **16** to pads **34** on its lower surface. Spring contact probes **60** providing tips for contacting I/O pads **28** may be formed on pads **34**. Alternatively spring contact probes **60** providing tips for contacting pads **34** may be formed on I/O pads **28**. Probes **60** are suitably designed to act as 50 Ohm transmission lines and are modeled as such in FIG. **4**.

As illustrated in FIG. **4**, the signal path through probe board assembly **58** linking node **16** to pads **34** includes a via **37** having a 50 Ohm characteristic impedance extending vertically downward from node **16** to a near 50 Ohm lumped impedance transmission line **32** implemented by a conductive trace on a layer of PCB **58**. One end of transmission line **32** is connected to node **16**. U.S. patent application Ser. No. 09/761,352 filed Jan. 16, 2001 (incorporated herein by reference) discloses methods for tuning the frequency response of a via, which may be used in conjunction with the instant invention. A set of isolation resistors **36** link taps **38** of transmission line **32** to a set of 50 Ohm vias **39** extending downward through probe board assembly **58** to the pads **34** on its lower surface. Thus a test signal generated by driver **24** travels over cable **55** and via **37** to transmission line **32**. Isolation resistors **36**, vias **39** and probes **60** then distribute the test signal to corresponding I/O pads **28** of four ICs **50**. FIG. **4** assumes that isolation resistors are embedded in probe board assembly **58** on the layer containing transmission line **32**, but they may be mounted on the upper surface of the probe board assembly. In such case, additional 50 Ohm vias (not shown) are provided to link taps **38** to isolation resistors **36**.

A defective IC may have a low impedance path from any I/O pad **28** to a ground, power or other conductor. When I/O pads **28** of several ICs were directly connected to one another, such a fault at any one I/O pad **28** would substantially affect the test signal voltage applied to all other pads **28** to which it is connected. Accordingly isolation resistors **36** are provided to isolate the I/O pads **28** of ICs **50** from one another so that a fault at an I/O pad **28** of a defective IC **50** will not substantially affect the voltage of the test signal arriving at I/O pads **28** of the other ICs **50** driven by the same test signal. Thus a fault at the I/O pad **28** of any defective IC **50** will not interfere with the tester's ability to test the other ICs.

The interconnect system of FIG. **4** is suitable for transmitting a low frequency test signal, however signal reflections occurring at each transmission line tap **38** can distort a high frequency test signal arriving at IC pads **28**. These test signal reflections occur as a result of discontinuity in signal path impedances at taps **38**. While the characteristic impedance of the transmission line **32** conveying the test signal into each tap **38** is 50 Ohms, the effective characteristic impedance of the signal paths conveying the test signal away from each tap **38** is the 40 Ohm parallel combination of the 50 Ohm transmission line **32** and a 50 Ohm isolation resistor **36**. The reflection occurs because the 50 Ohm input impedance at each tap **38** does not match the 40 Ohm output impedance. These reflections are undesirable because they appear as distortions in the test signal as it arrives at IC I/O pads **28**. The impedance mismatch at taps **38** can worsen when isolation resistors **36** do not reside on the same layer as transmission line **32** and vias are needed to link each tap **38** to an isolation resistor **36**.

Since the magnitude of the reflection at each tap depends on the magnitude of the impedance mismatch, we reduce the reflection by increasing the size of isolation resistors **36**, thereby decreasing the impedance mismatch. For example if resistors **36** were 400 Ohms each, then the output impedance of each tap **38** would be the parallel combination of 50 Ohms and 400 Ohms (about 44.5 Ohms) which would produce a smaller reflection at the tap. However increasing the size of isolation resistors **36** has a cost. In order to change the state of a test signal appearing at any IC I/O pad **28**, it is necessary for the test signal to charge or discharge the capacitance **26** at the pad. By increasing the size of isolation resistors **36**, we also increase the time the test signal needs to charge or discharge capacitance **26** at I/O pads **28** when it changes state. Since tester **10** has to wait longer between test signal state changes, it takes longer for it to test the ICs.

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FIG. 5 illustrates another exemplary embodiment of the invention for distributing a test signal to several I/O pads **28**, which reduces the reflection problem and minimizes differences in test signal voltages and edge timing at the I/O pads. The test signal from a driver **24** in tester **10** travels to connector node **16** on probe board assembly **58** through the 50 Ohm coaxial cable (or pogo pin) **55**. The test signal then passes downward through a 50 Ohm via **40** to a node **41** residing on a layer of the probe board assembly containing two 100 Ohm transmission lines **42**. The two transmission lines **42** convey the test signal from node **41** to two nodes **43**, and four 50 Ohm transmission lines **44** convey the test signal from nodes **43** to a set of four 50 Ohm isolation resistors **45**. 50 Ohm vias **46** route the test signal downward to pads **34** on the lower surface of probe board assembly **58**, and four 50 Ohm spring contact probes **60** link pads **34** to the I/O pads **28** of four ICs on wafer **14**.

No test signal reflection occurs at node **41** because the parallel combination of two 100 Ohm transmission lines **42** conveying the test signal away from node **41** matches the impedance of the 50 Ohm via **40** conveying the signal into node **41**. Similarly no test signal reflections occur at nodes **43** because the parallel combination of 50 Ohm impedances of the transmission lines **44** carrying the test signal away from each node **43** matches the 100 Ohm impedance of the transmission line **42** delivering the test signal into each node **43**. Since all components of the signals paths downstream of nodes **42** are 50 Ohms there are no test signal reflections at the junctions of those components. A test signal reflection does occur at each I/O contact **28**, but since that reflection is downstream of an isolation resistor **45**, it is largely absorbed by the isolation resistor and does not substantially distort the test signal on the upstream side of the isolation resistor. Therefore a test signal reflection at any one I/O pad **28** is severely attenuated before it reaches any other I/O pad **28**.

The tree-like test signal distribution system illustrated in FIG. 5 has several advantages over the tapped distribution system of FIG. 4. While reflections in the distribution network of FIG. 4 can substantially distort the test signal arriving at each pad **28**, reflections in the distribution network of FIG. 5 are substantially attenuated before they have a significant effect elsewhere in the network. While in the network of FIG. 4 a test signal edge arrives at each pad **28** at a different time, in the network of FIG. 5 each test signal edge can arrive at all pads **28** at substantially the same time when path lengths of the corresponding transmission lines are suitably matched. Also while the network of FIG. 4 delivers the test signal to each pad **28** with a different voltage, the network of FIG. 5 delivers the test signal with substantially the same voltage to all pads **28**.

However the test signal distribution network of FIG. 5 requires probe board assembly **58** to provide transmission lines and vias having a variety of characteristic impedances ranging from 50 to 200 Ohms. The characteristic impedance of a trace formed on a substrate is a function of a number of factors including the width of the trace, distances to nearby ground or power conductors, and the dielectric constant of substrate separating the trace from nearby ground and power conductors. The characteristic impedance of a via is primarily a function of its physical dimensions, distances to nearby ground and power conductors and the dielectric constant of the PCB substrate surrounding it. The signal distribution architecture illustrated in FIG. 5 is therefore more difficult to design and expensive to fabricate a probe board assembly providing transmission lines having a variety of characteristic impedances than a probe board assem-

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bly in which all transmission lines have the same characteristic impedance. Also in the context of a probe board assembly wherein large numbers of transmission lines must be packed into a small volume it is less practical to provide transmission lines having characteristic impedances above 100–150 ohms because high impedance transmission lines take up too much space. Signal conductors forming higher impedance transmission lines must be more widely separated from ground and power conductors.

FIG. 6 is a schematic diagram illustrating an example of how probe board assembly **58** of FIG. 3A or 3B may implement a signal path in accordance with the invention for distributing a single test signal to I/O pads **78** of four ICs **50**. The primarily capacitive input impedance (typically 2 picofarads) of each I/O pad **78** is represented in FIG. 4 by a capacitor **80**.

Referring to FIGS. 3A, 3B and 6, a driver **62** within IC tester **54** transmits a test signal through a coaxial cable **55** or pogo pin **57** to an entry node **63** of probe board assembly **58**. In this example, where driver **62** has a 50 Ohm output impedance, a 50 Ohm coaxial cable **55** or pogo pin **57** is employed to convey the signal between the driver and entry node **63**. FIG. 4 therefore depicts coaxial cable **55** or pogo pin **57** as a 50 Ohm transmission line. A 50 Ohm transmission line **64** provided by probe board assembly **58** conveys the test signal to a "branch node" **66** at a junction between four 200 Ohm isolation resistors **67**. Transmission line **64** is formed by horizontal traces residing on layers of probe board assembly **58** and vias passing vertically though layers of the probe board assembly. When the layers of the probe board assembly **58** include substrates that are vertically spaced from one another, transmission line **64** may also include spring contacts or other conductors extending between the spaced layers.

Each isolation resistor **67** links branch node **66** to one end of a separate one of a set of 50 Ohm transmission lines **68**, each of which conveys the TEST signal to a separate pad **74** formed on the lower side of probe board assembly **58**. Each transmission line **68** may include horizontal traces residing on layers of probe board assembly **58**, vias passing vertically though layers of the probe board assembly and from one another, transmission line **64** may also include spring contacts or other conductors extending between the layers when the layers are spaced apart. A set of 50 Ohm probes **60** provide signal paths between the pads **74** and the IC I/O pads **78**.

Isolation resistors **67** isolate the I/O pads **78** of ICs **50** from one another so that a fault such as a low impedance path to ground, power or another signal conductor at any I/O pad **78** of a defective IC **50** will not substantially affect the test signal voltage applied to other I/O pads **78** driven by the same test signal. Thus a fault at the I/O pad **78** of any one defective IC **50** will not interfere with the tester's ability to test other ICs.

The four isolation resistors **67** are mounted on a layer of probe board assembly **58** with their ends close to branch node **66** so that the branch node acts as a single junction between the 50 Ohm transmission line **65** and the four 200 Ohm resistors **67**. Thus a test signal entering branch node **66** through the 50 Ohm transmission line **65** encounters a parallel combination of four 200 Ohm resistors **67**, which is the equivalent of 50 Ohms. There may be some signal reflection from node **78** back toward node **82**, however the effect of any such reflection may be minimized by keeping the transit time between nodes **82** and **78** relatively short as compared to the rise time of the signal. Such reflections may

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be reduced or eliminated by terminating node 78 with a 50 ohm resistor. In such a case, the drive level voltage from the tester driver 62 may be increased to compensate for a voltage drop across the 50 ohm resistor.

The test signal distribution network illustrated in FIG. 4 does, however, include eight points at which a mismatch in input and output impedance do lead to test signal reflections. There is an impedance mismatch at each of the four nodes 82 at the junction between each 200 Ohm isolation resistor 67 and one of 50 Ohm transmission lines 68. There is also an impedance mismatch at each of the four IC I/O pads 78 where a 50 Ohm probe 60 meets the 2 picofarad input capacitance 80 of the pad. But note that each impedance mismatch point 78 or 82 at which a reflection occurs is downstream of one of the 200 Ohm isolation resistors 67. Each isolation resistor 67 greatly attenuates the reflections occurring downstream so that they have very little effect on the test signal upstream of the isolation resistor. Thus a test signal reflection occurring in any branch of the network leading to any one I/O IC pad 78 has little distorting effect on the test signal passing though a branch of the network leading to any other IC I/o pad 78.

Comparing the test signal distribution networks of FIGS. 4 and 5 to the distribution network of FIG. 6, note that the networks of FIGS. 5 and 6 both substantially reduce test signal distortion due to reflections over that occur in the network of FIG. 2. Note also that unlike the test signal distribution network of FIG. 4, it is possible to balance the networks of FIGS. 5 and 6 so that each test signal edge will arrive at all I/O pads 78 at substantially the same time and with substantially the same amount of attenuation.

Unlike the test signal distribution networks of FIG. 5, the network of FIG. 6 permits all traces 65 and 68 and all vias 64 and 69 to have the same characteristic impedance. This makes a probe board assembly 58 implementing the network of FIG. 6 easier to design and less costly to manufacture than a probe board assembly 20 implementing the network of FIG. 5, which would have to provide transmission lines having a variety of characteristic impedances.

Thus the branching signal path of FIG. 6 provides resistors at the branch points of a branching network within a probe board assembly to deliver a test signal to several ICs. It should be understood that many variations to the topology of a branching network of FIG. 6 are possible. For example given an 50 Ohm transmission line conveying a test signal to a branch point, a set of six 300 Ohm isolation resistors linked to the branch point could distribute the test signal to six ICs, or a set of eight 400 Ohm isolation resistors at the branch point could distribute the signal to eight ICs. The transmission lines 55, 57, 64, 69 and probes 60 may be other than 50 Ohms. For example when all transition lines and probes are 75 Ohms, resistors 67 may be 300 Ohms. It is not necessary that all transmission lines and probes have the same characteristic impedance. For example while transmission line 55, 57 and 64 should have a matching impedance of for example 50 Ohms, transmission lines 68 and probes 60 may have, for example, a 100 Ohm impedance that does not match that of transmission lines 55, 57 and 64.

A signal path through probe board assembly 58 of FIG. 3A or 3B may include more than one branch point. For example FIG. 7 illustrates an exemplary embodiment of the invention, a network having three branch points 82, 84 and 86, wherein at each branch point a 50 Ohm transmission line branches into two 100 Ohm isolation resistors and. 50 Ohm transmission lines convey the test signal to the IC pads. Note that each impedance discontinuity in which a 100 Ohm

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resistor meets a single 50 Ohm transmission line occurs downstream of a 100 Ohm resistor which can substantially dissipate the energy of reflections occurring at the discontinuity.

FIG. 8 illustrates a branching path within a probe board assembly implemented in accordance with another exemplary embodiment of the invention wherein a 50 Ohm transmission line branches into two 100 Ohm transmission lines at a branch point 88. Each of the two 100 Ohm transmission lines then branches into two 200 Ohm resistors at branch points 90 and 92. 50 Ohm transmission lines convey the test signals from the 200 Ohm resistors to the IC pads. This embodiment of the invention requires the probe board assembly to implement both 50 Ohm and 100 Ohm transmission lines. However while transmission lines having characteristic impedances much larger than about 150 Ohms are difficult to implement on PCBs, it 50 and 100 Ohm transmission lines can be easily implemented.

FIG. 9 illustrates another exemplary embodiment of the invention, a multiple-layer probe card assembly 120 for providing signal paths between an integrated circuit tester 122 and pads 123 on surfaces of IC dice 124 on a wafer 126 under test. Probe card assembly 120 includes a probe board 130 having a set of pads 132 on its upper surface for receiving tips of a set of pogo pin connectors 134 providing signal paths between tester 122 and pads 132. An interposer layer 135 having a set of spring contacts 136 and 138 connected to its upper and lower surfaces provides signal paths between a set of contacts 140 on the lower surface of probe board 130 and a set of contacts 142 on an upper surface of a space transformer board 144. A set of probes 146 provide signal paths between pads 148 on the lower surface of space transformer 144 and IC pads 123. Probe board 130, interposer 138 and space transformer 144 may include single or multiple insulating substrates with traces formed on the substrates and vias extending through the substrate for conducting signals horizontally and vertically between pads and/or contacts on their upper and lower surfaces. In other embodiments of the invention, cables may be used to link tester 122 to probe board 130 in lieu of pogo pins 136.

In accordance with this exemplary embodiment of the invention, some of the signal paths though probe board assembly 120 branch so that a channel of IC tester 122 employing a single one of pogo pins 134 as an output terminal can concurrently drive more than one IC pad 123. Isolation resistors (not shown in FIG. 15) formed on or within one or more of layers 130, 135 and 144 are included in the branching paths between pogo pins 134 and IC pads 123.

FIGS. 10–13 are schematic diagrams illustrating various exemplary embodiments of a branching signal path within probe board assembly 120 in accordance with the invention. In FIG. 10 the isolation resistors 150 are formed on or between layers of probe board 130. In the examples of FIGS. 11 and 12, the isolation resistors 150 are formed on or between layers of interposer 135 and space transformer 134, respectively. A hierarchical resistor network (such as illustrated in FIGS. 5–7) may also be implemented by mounting resistors on one or more boards of probe board assembly 120. For example, FIG. 19 illustrates a signal path including such a hierarchy including isolation resistors 150 formed on probe board 130 and on space transformer 134.

While exemplary embodiments of an interconnect systems in accordance with the invention described herein above provide a branching signal paths between an IC tester and I/O pads of one or more ICs 50 that have not yet been

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separated from the semiconductor wafer **52** on which they are formed, similar branching signal paths can be provided in interconnect systems that linking IC testers to ICs after they have been separated from one another. For example, arrays of separated, unpackaged ICs held in trays can be concurrently accessed by the same IC tester using interconnect systems generally similar to that described above. When the ICs are packaged, the probes may be adapted access package pins or other types of IC package terminals I/O pads on the surface of the ICs.

The forgoing specification and the drawings depict the best mode(s) of practicing the invention, and elements or steps of the depicted best mode(s) exemplify the elements or steps of the invention as recited in the appended claims. However the appended claims are intended to apply to any mode of practicing the invention comprising the combination of elements or steps as described in any one of the claims, including elements or steps that are functional equivalents of the example elements or steps depicted in the specification and drawings.

What is claimed is:

1. An apparatus for providing signal paths between an integrated circuit (IC) tester and a plurality of IC terminals so that a driver within the IC tester can concurrently transmit a test signal to the IC terminals, said test signal exhibiting high and low voltage levels representing logic states, wherein a fault at any one of the IC terminals conductively linking that IC terminal to a source of potential can drive that IC terminal near either of said high and low voltage levels, the apparatus comprising:

   a first signal path having a first characteristic impedance for conveying the test signal away from the driver;

   a plurality of probes, each for conveying the test signal to a separate one of the plurality of IC terminals; and

   a network comprising resistors for conveying the test signal from the first signal path to each of the probes,

   wherein the resistors isolate the IC terminals from one another by an amount of resistance that is substantially larger than the first characteristic impedance of the first signal path and sufficiently large to prevent the fault at any one of the IC terminals from affecting a logic state represented by the test signal at any other of the IC terminals.

2. The apparatus in accordance with claim **1** wherein the first signal path and the probes have substantially similar characteristic impedances.

3. The apparatus in accordance with claim **1** wherein the network comprises:

   a second signal path having a set of taps, the first signal path delivering the test signal to the second signal path, the second signal path conveying the test signal to its taps;

   a plurality of first resistors, each having a first terminal connected to a separate one of said taps for receiving the test signal, and having a second terminal, each first resistor conveying the test signal from its first terminal to its second terminal; and

   a plurality of third signal paths, each conveying the test signal from a separate one of the second terminals to a separate one of the probes.

4. The apparatus in accordance with claim **3** wherein the second signal path has a uniform second characteristic impedance between its taps substantially matching the first characteristic impedance of the first signal path.

5. The apparatus in accordance with claim **1** wherein the network comprises:

   a first node (**41**), the first signal path delivering the test signal to the first node;

   a plurality of second nodes (**43**);

   a plurality of second signal paths (**42**), each connected for conveying the test signal from the first node to a separate one of the second nodes, and each second signal path having a second characteristic impedance;

   a plurality of first resistors;

   a plurality of sets of third signal paths (**44**), each set corresponding to a separate one of the second nodes, each third signal path of each set being connected for conveying the test signal from the set's corresponding second node to a separate one of the first resistors, and each third signal path having a third characteristic impedance.

6. The apparatus in accordance with claim **5** wherein the second characteristic impedances of the second signal paths are sized relative to the first characteristic impedance of the first signal path so as to substantially minimize test signal reflections at the first node.

7. The apparatus in accordance with claim **6** wherein the third characteristic impedances of the third signal paths are sized relative to the second characteristic impedance of the second signal path so as to substantially minimize test signal reflections at the second nodes.

8. The apparatus in accordance with claim **1** wherein the network comprises:

   a first node (**66**), the first signal path delivering the test signal to the first node;

   a plurality of first resistors (**67**), each having a first terminal and a second terminal, the first terminals of all first resistors being connected to the first node such that each resistor conveys the test signal from the first node to its second terminal, and

   a plurality of second signal paths (**68**), each linking the second terminal of a separate one of the first resistors to a separate one of the probes.

9. The apparatus in accordance with claim **8** wherein the first resistors are of resistances sized relative to the first characteristic impedance of the first signal path so as to substantially minimize test signal reflections at said first node.

10. The apparatus in accordance with claim **1** wherein the network comprises:

   a first node (**82**), the first signal path delivering the test signal to the first node;

   a plurality of first resistors, each having a first terminal and a second terminal, the first terminals of all first resistors being connected to the first node such that each first resistor conveys the test signal from the first node to its second terminal,

   a plurality of second nodes (**84, 86**);

   a plurality of second signal paths, each having a second characteristic impedance and being linked for conveying the test signal from the first node to a separate one of the second nodes;

   a plurality of sets of second resistors, each set corresponding to a separate one of the second nodes, each second resistor having a third terminal and a fourth terminal, the third terminals of the second resistors of each set being connected to the set's corresponding second node; and

   a plurality of third signal paths, each third signal path being connected for conveying the test signal from the

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second terminal of a separate one of the first resistors to a separate one of the probes.

11. The apparatus in accordance with claim 10 wherein the first resistors are of resistances sized relative to the first characteristic impedance of the first signal path so as to substantially minimize test signal reflections at the first node.

12. The apparatus in accordance with claim 11 wherein the second resistors are of resistances sized relative to the second characteristic impedances of the second signal paths so as to substantially minimize test signal reflections at the second nodes.

13. The apparatus in accordance with claim 11 wherein the first, second and third signal paths all have substantially similar impedances.

14. The apparatus in accordance with claim 1 wherein the network comprises:
  a first node (88), the first signal path delivering the test signal to the first node;
  a plurality of second nodes (90, 92);
  a plurality of second signal paths (42), each having a second characteristic impedance being connected for conveying the test signal from the first node to a separate one of the second nodes;
  plurality of sets of first resistors, each set corresponding to a separate one of the second nodes, each first resistor having a first terminal and a second terminal, the first terminals of all first resistors of each set being to a corresponding one of the second nodes; and
  a plurality of third transmission lines, each for conveying the test signal from the second terminal of a separate one of the first resistors to a separate one of the probes.

15. The apparatus in accordance with claim 14 wherein the second characteristic impedances of the second signal paths are sized relative to the first impedance of the first signal path to substantially minimize test signal reflections at the first node.

16. The apparatus in accordance with claim 15 wherein a resistance of each first resistor is sized to substantially minimize test signal reflections the second nodes.

17. The apparatus in accordance with claim 1 wherein said first characteristic impedance is less than 150 Ohms.

18. The apparatus in accordance with claim 1 wherein said first characteristic impedance is in a range of 50 to 150 Ohms.

19. An apparatus for providing signal paths between an integrated circuit (IC) tester and a plurality of IC terminals so that a driver within the IC tester can concurrently transmit a test signal to the IC terminals, said test signal exhibiting high and low voltage levels representing logic states, wherein a fault at any one of the IC terminals conductively linking that IC terminal to a source of potential can drive that IC terminal near either of said high and low voltage levels, the apparatus comprising:
  a first signal path having a first characteristic impedance for conveying the test signal away from the driver;
  a plurality of probes, each for conveying the test signal to a separate one of the plurality of IC terminals; and
  a probe board assembly comprising:
    at least one substrate; and
    a network comprising resistors supported by the at least one substrate, for conveying the test signal from the first signal path to each of the probes,
    wherein the resistors isolate the IC terminals from one another by an amount of resistance that is substantially larger than the first characteristic impedance of

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the first signal path and sufficiently large to prevent the fault at any one of the IC terminals from affecting a logic state represented by the test signal at any other of the IC terminals.

20. The apparatus in accordance with claim 19 wherein the probes are attached to the probe board assembly and include tips for contacting the IC terminals.

21. The apparatus in accordance with claim 19 wherein the probes are attached to the IC terminals and include tips for contacting the probe board assembly.

22. The apparatus in accordance with claim 19 wherein the network comprises:
  a second signal path having a set of taps, the first signal path delivering the test signal to the second signal path, the second signal path conveying the test signal to its taps, wherein the second signal path has a uniform second characteristic impedance between its taps substantially matching the first characteristic impedance of the first signal path;
  a plurality of first resistors, each having a first terminal connected to a separate one of said taps for receiving the test signal, and having a second terminal, each first resistor conveying the test signal from its first terminal to its second terminal; and
  a plurality of third signal paths, each conveying the test signal from a separate one of the taps to a separate one of the probes.

23. The apparatus in accordance with claim 19 wherein the network comprises:
  a first node (41), the first signal path delivering the test signal to the first node;
  a plurality of second nodes (43);
  a plurality of second signal paths (42), each connected for conveying the test signal from the first node to a separate one of the second nodes, and each second signal path having a second characteristic impedance sized relative to the first characteristic impedance of the first signal path so as to substantially minimize test signal reflections at the first node;
  a plurality of first resistors;
  a plurality of sets of third signal paths (44), each set corresponding to a separate one of the second nodes, each third signal path of each set being connected for conveying the test signal from the set's corresponding second node to a separate one of the first resistors, and each third signal path having a third characteristic impedance sized relative to the second characteristic impedance of the second signal path so as to substantially minimize test signal reflections at the second nodes.

24. The apparatus in accordance with claim 19 wherein the network comprises:
  a first node (66), the first signal path delivering the test signal to the first node;
  a plurality of first resistors (67), each having a first terminal and a second terminal, the first terminals of all first resistors being connected to the first node such that each resistor conveys the test signal from the first node to its second terminal, wherein the first resistors are of resistances sized relative to the first characteristic impedance of the first signal path so as to substantially minimize test signal reflections at said first node, and
  a plurality of second signal paths (68), each linking the second terminal of a separate one of the first resistors to a separate one of the probes.

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25. The apparatus in accordance with claim **19** wherein the network comprises:

a first node (**82**), the first signal path delivering the test signal to the first node;

a plurality of first resistors, each having a first terminal and a second terminal, the first terminals of all first resistors being connected to the first node such that each first resistor conveys the test signal from the first node to its second terminal,

a plurality of second nodes (**84, 86**);

a plurality of second signal paths, each having a second characteristic impedance and being linked for conveying the test signal from the first node to a separate one of the second nodes;

a plurality of sets of second resistors, each set corresponding to a separate one of the second nodes, each second resistor having a third terminal and a fourth terminal, the third terminals of the second resistors of each set being connected to the set's corresponding second node; and

a plurality of third signal paths, each third signal path being connected for conveying the test signal from the second terminal of a separate one of the first resistors to a separate one of the probes,

wherein the first resistors are of resistances sized relative to the first characteristic impedance of the first signal path so as to substantially minimize test signal reflections at the first node, and

wherein the second resistors are of resistances sized relative to the second characteristic impedances of the second signal paths so as to substantially minimize test signal reflections at the second nodes.

26. The apparatus in accordance with claim **19** wherein the network comprises:

a first node (**88**), the first signal path delivering the test signal to the first node;

a plurality of second nodes (**90, 92**);

a plurality of second signal paths (**42**), each being connected for conveying the test signal from the first node

to a separate one of the second nodes, and each having a second characteristic impedances sized relative to the first impedance of the first signal path to substantially minimize test signal reflections at the first node,

a plurality of sets of first resistors, each set corresponding to a separate one of the second nodes, each first resistor having a first terminal and a second terminal, the first terminals of all first resistors of each set being to a corresponding one of the second nodes, wherein a resistance of each first resistor is sized to substantially minimize test signal reflections the second nodes; and

a plurality of third transmission lines, each for conveying the test signal from the second terminal of a separate one of the first resistors to a separate one of the probes.

27. The apparatus in accordance with claim **19** wherein said first characteristic impedance is less than 150 Ohms.

28. The apparatus in accordance with claim **19** wherein said first characteristic impedance is in a range of 50 to 150 Ohms.

29. The apparatus in accordance with claim **19**,

wherein said probe board assembly comprises a printed circuit board having a plurality of layers,

wherein said network comprises said resistors and traces formed on at least one layer of the printed circuit board and vias passing though the layers of the printed circuit board, and

wherein all said traces and vias forming the network have substantially similar characteristic impedances.

30. The apparatus in accordance with claim **19**

wherein said probe board assembly comprises a plurality of substrates spaced apart from one another, and

wherein the network comprises conductors extending between and conveying the test signal through of the substrates.

31. The apparatus in accordance with claim **30** wherein the resistors are mounted on only one of the substrates.

32. The apparatus in accordance with claim **30** wherein the resistors are mounted on more than one of the substrates.

*   *   *   *   *